FPD-Link Demonstration Kit User Manual

P/N: FLINK3V10BT-TX/RX

Rev 0.6

Flat Panel Displays

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Introduction:

National Semiconductor's Flat Panel Displays FPD-Link evaluation kit contains a Transmitter (Tx) board, a Receiver (Rx) board along with interfacing cables. This kit will demonstrate the chipsets interfacing from test equipment or a graphics controller using Low Voltage Differential Signaling (LVDS) to a receiver board. The DS90C3201 and DS90C3202 are a 10-bit color Transmitter and Receiver chipset designed to transmit data at clocks speeds from 8 to 135 MHz. Using a 10-bit color depth system, the 30-bit RGB color produces over 1.07 billion colors to represent high definition displays in their most natural color. The dual high speed LVDS channels supports single pixel in-single pixel out and dual pixel in-dual pixel out transmission modes.

The Transmitter board accepts LVTTL/LVCMOS RGB signals from the graphics controller along with the clock signal. The LVDS Transmitter converts the LVTTL/LVCMOS parallel lines into ten serialized LVDS data pairs plus a LVDS clock. The serial data streams toggle at 3.5 times the clock rate. With an input clock at 135 MHz, the maximum transmission rate of each LVDS line is 945Mbps, for an aggregate throughput rate of 9.45Gbps. This allows the 10-bit color LVDS Receiver to support resolutions up to HDTV.

The Receiver board accepts the LVDS serialized data streams plus clock and converts the data back into parallel LVTTL/LVCMOS RGB signals and clock for the panel timing controller.

The user needs to provide the proper RGB inputs and clock to the Transmitter and also provide a proper interface from the Receiver output to the LCD panel or test equipment. The transmitter and receiver boards can be used to evaluate device parameters. A cable conversion board or harness scramble may be necessary depending on type of cable/connector interface used. A power down feature is also provided that reduces current draw when the link is not required. Other device features and configurations can be programmed via 2-wire serial interface

Contents of the Evaluation Kit:

1) One Transmitter board with the DS90C3201
2) One Receiver board with the DS90C3202
3) One 50-pin IDC Flat Ribbon Cable
4) Evaluation Kit Documentation (this manual)
5) DS90C3201/3202 Datasheet

FPD-Link Typical Application:

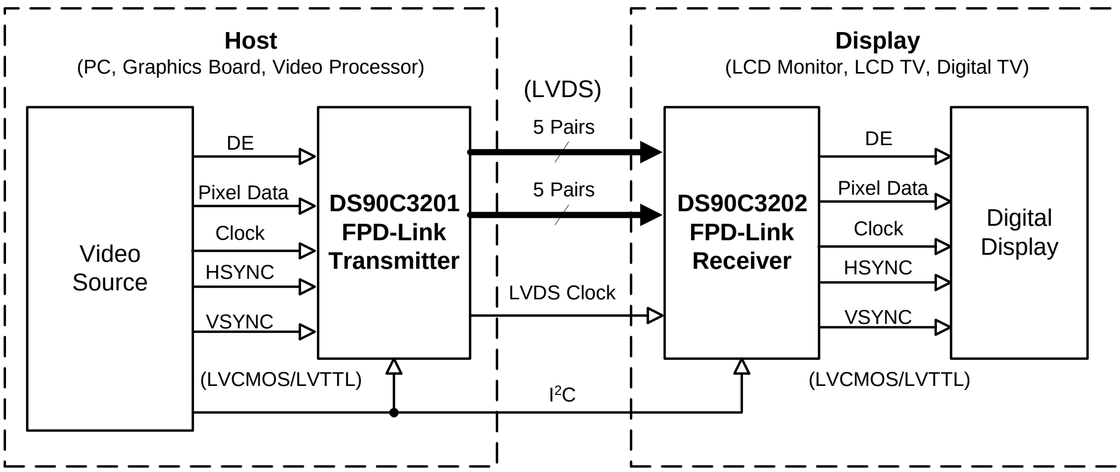


Figure 1a. Typical FPD-Link Application (Dual 30-bit RGB Color)

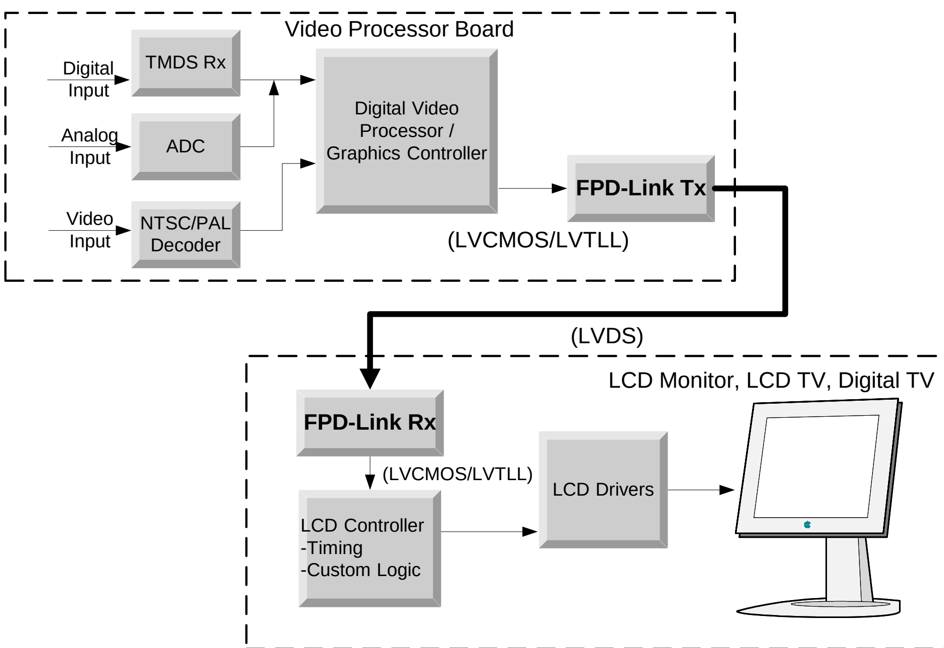


Figure 1b. Typical FPD-Link System Diagram

The diagrams above illustrate the use of the Chipset (Tx/Rx) in a Host to Flat Panel Interface.

Chipsets support up to 18-bit, 24-bit, and 30-bit color depth TFT LCD Panels for any VGA (640X480), SVGA (800X600), XGA (1024X768), WXGA (1280X768) SXGA (1280X1024), SXGA+ (1400X1050), HDTV (1920X1080) resolutions.

Refer to the proper datasheet information on Chipsets (Tx/Rx) provided on each board for more detailed information.

How to set up the Evaluation Kit:

The PCB routing for the Tx input pins (TxIN) have been laid out to accept incoming data from IDC connectors. The TxOUT/RxIN interface uses a 50-pin IDC connector through a IDC ribbon cable. Please follow these steps to set up the evaluation kit for bench testing and performance measurements:

1) Connect one end of the 50-pin IDC cable to the transmitter board and the other end to the receiver board. Longer lengths can be used.

2) Jumpers and switches have been configured at the factory; they should not require any changes for operation of the chipset. See text on Configuration settings for more details.

3) From the Video Decoder board, connect a flat cable (not supplied) to the transmitter board and connect another flat cable (not supplied) from the receiver board to the panel (Note: Refer Page 19 for suggested mapping schemes). A scramble cable may be required.

4) Power for the Tx and Rx boards must be supplied externally through Power Jack (VDD). Grounds for both boards are connected through Power Jack (VSS) (see section below).

5) 2-wire serial interface for external EEPROM circuitry power is supplied through Power jack (VDDE) and Ground for Power Jack (VSSE).

Power Connection:

The Transmitter and Receiver boards must be powered by supplying power externally through J2 (VDD) and J3 (VSS) on Transmitter Board and J4 (VDD) and J5 (VSS) on Receiver board. The maximum voltage that should ever be applied to the FPD-Link Transmitter (DS90C3201) or Receiver (DS90C3202) VDD terminal is +4V MAXIMUM. Optional EEPROM circuitry power is supplied through J4 (VDDE), J5 (VSSE) or JP79 on Transmitter Board and J2 (VDDE), J3 (VSSE) or JP74 on Receiver Board.

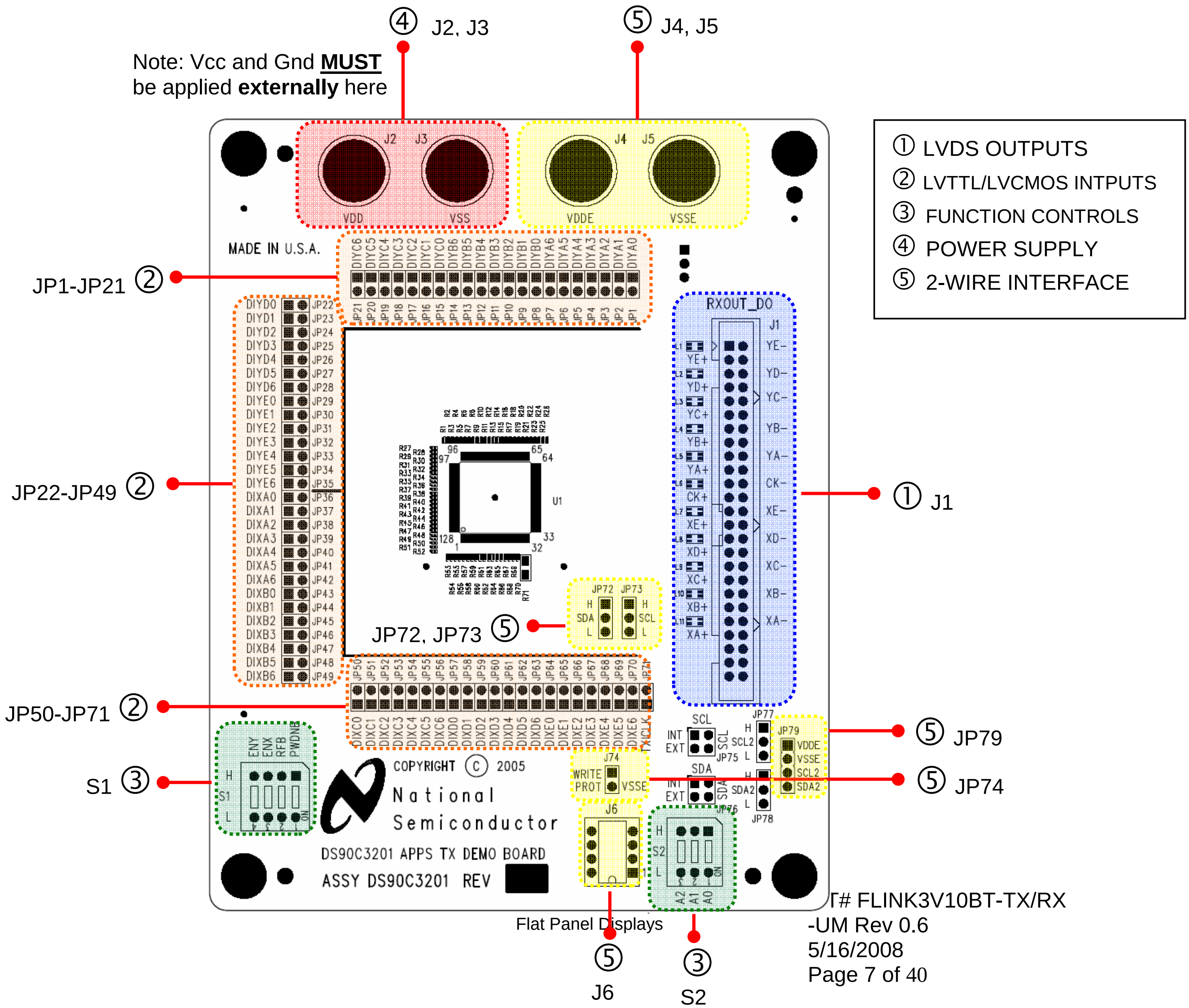
FPD-Link Transmitter Board Description:

JP1 to JP71 IDC connectors accepts 70 bits of LVTTL/LVCMOS RGB data along with the clock input.

The FPD-Link Transmitter board is powered externally from the J2 and J3 connectors shown below. For the transmitter to be operational, the Power Down (PWDN) switch on S2 must be set HIGH. Rising or falling edge reference clock is also selected by S2 tied to HIGH (rising) or LOW (falling). Other device features and configurations can be programmed via 2-wire serial interface through JP79.

The 50-pin IDC connector (J1) provides the interface for LVDS signals for the Receiver board.

TDK EMC common-mode filters have been added in series on the LVDS signals for high-frequency noise suppression.



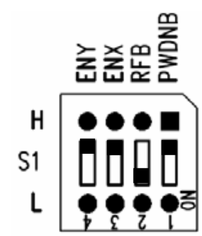
Configuration Settings for the Tx Board

Reference	Description	Open	Closed
WRITE PORT (J74)	2-wire Serial Interface Write Protect	Write Enabled	Write-Protected

Default setting for J74 is set Open (to VSS), Write Enabled.

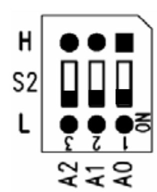
S1: Transmitter Features Selection

Reference	Description	L	H	S1
ENY ***(MODE1)***	**EN**able "**Y**" Bank *"ODD" Data Channels*	Disabled	Enabled (Default)	
ENX ***(MODE0)***	**EN**able "**X**" Bank *"EVEN" Data Channels*	Disabled	Enabled (Default)	
RFB	**R**ising or **F**alling Data Strobe	Falling (Default)	Rising	
PWDNB	**P**o**W**er**D**ow**N** **B**ar	Powers Down	Operational (Default)	



S2: External EEPROM Slave Address

Reference	Description	S2
A2	Slave Address A2 (Default LOW)	
A1	Slave Address A1 (Default LOW)	
A0	Slave Address A0 (Default LOW)	



Default setting for S2 is set to all LOW, External EEPROM Slave Address A[2:0]=000

Tx LVTTL/LVCMOS and LVDS Pinout by IDC Connector

The following two figures illustrate how the Tx inputs are mapped to the IDC connectors J1P to JP71 (Note – labels are also printed on the demo boards). The LVDS outputs for the 50-pin IDC (J1) connector pinout are also shown.

BANK X INPUTS EVEN Data Channels		BANK Y INPUTS ODD Data Channels	
Pin No.	Symbol REF **(Pin Name)**	Pin No.	Symbol REF **(Pin Name)**
JP36	DIXA0 **(TXEE0)**	JP1	DIYA0 **(TXOE0)**
JP37	DIXA1 **(TXEE1)**	JP2	DIYA1 **(TXOE1)**
JP38	DIXA2 **(TXEE2)**	JP3	DIYA2 **(TXOE2)**
JP39	DIXA3 **(TXEE3)**	JP4	DIYA3 **(TXOE3)**
JP40	DIXA4 **(TXEE4)**	JP5	DIYA4 **(TXOE4)**
JP41	DIXA5 **(TXEE5)**	JP6	DIYA5 **(TXOE5)**
JP42	DIXA6 **(TXEE6)**	JP7	DIYA6 **(TXOE6)**
JP43	DIXB0 **(TXED0)**	JP8	DIYB0 **(TXOD0)**
JP44	DIXB1 **(TXED1)**	JP9	DIYB1 **(TXOD1)**
JP45	DIXB2 **(TXED2)**	JP10	DIYB2 **(TXOD2)**
JP46	DIXB3 **(TXED3)**	JP11	DIYB3 **(TXOD3)**
JP47	DIXB4 **(TXED4)**	JP12	DIYB4 **(TXOD4)**
JP48	DIXB5 **(TXED5)**	JP13	DIYB5 **(TXOD5)**
JP49	DIXB6 **(TXED6)**	JP14	DIYB6 **(TXOD6)**
JP50	DIXC0 **(TXEC0)**	JP15	DIYC0 **(TXOC0)**
JP51	DIXC1 **(TXEC1)**	JP16	DIYC1 **(TXOC1)**
JP52	DIXC2 **(TXEC2)**	JP17	DIYC2 **(TXOC2)**
JP53	DIXC3 **(TXEC3)**	JP18	DIYC3 **(TXOC3)**
JP54	DIXC4 **(TXEC4**)	JP19	DIYC4 **(TXOC4**)
JP55	DIXC5 **(TXEC5)**	JP20	DIYC5 **(TXOC5)**
JP56	DIXC6 **(TXEC6)**	JP21	DIYC6 **(TXOC6)**
JP57	DIXD0 **(TXEB0)**	JP22	DIYD0 **(TXOB0)**
JP58	DIXD1 **(TXEB1)**	JP23	DIYD1 **(TXOB1)**
JP59	DIXD2 **(TXEB2)**	JP24	DIYD2 **(TXOB2)**
JP60	DIXD3 **(TXEB3)**	JP25	DIYD3 **(TXOB3)**
JP61	DIXD4 **(TXEB4)**	JP26	DIYD4 **(TXOB4)**
JP62	DIXD5 **(TXEB5)**	JP27	DIYD5 **(TXOB5)**
JP63	DIXD6 **(TXEB6)**	JP28	DIYD6 **(TXOB6)**
JP64	DIXE0 **(TXEA0)**	JP29	DIYE0 **(TXOA0)**
JP65	DIXE1 **(TXEA1)**	JP30	DIYE1 **(TXOA1)**
JP66	DIXE2 **(TXEA2)**	JP31	DIYE2 **(TXOA2)**
JP67	DIXE3 **(TXEA3)**	JP32	DIYE3 **(TXOA3)**
JP68	DIXE4 **(TXEA4)**	JP33	DIYE4 **(TXOA4)**
JP69	DIXE5 **(TXEA5)**	JP34	DIYE5 **(TXOA5)**
JP70	DIXE6 **(TXEA6)**	JP35	DIYE6 **(TXOA6)**
JP71		TXCLK **(TCLKIN)**	

LVDS OUTPUTS (J1)			
ODD Data Channels		EVEN Data Channels	
Pin No.	Symbol REF **(Pin Name)**	Pin No.	Symbol REF **(Pin Name)**
1	GND	26	XE - **(TXEA-)**
2	YE - **(TXOA-)**	27	XE+ **(TXEA+)**
3	YE+ **(TXOA+)**	28	GND
4	GND	29	GND
5	GND	30	XD - **(TXEB-)**
6	YD - **(TXOB-)**	31	XD+ **(TXEB+)**
7	YD+ **(TXOB+)**	32	GND
8	GND	33	GND
9	GND	34	XC - **(TXEC-)**
10	YC - **(TXOC-)**	35	XC+ **(TXEC+)**
11	YC+ **(TXOC+)**	36	GND
12	GND	37	GND
13	GND	38	XB - **(TXED-)**
14	YB - **(TXOD-)**	39	XB+ **(TXED+)**
15	YB+ **(TXOD+)**	40	GND
16	GND	41	GND
17	GND	42	XA - **(TXEA-)**
18	YA - **(TXOE-)**	43	XA+ **(TXEA+)**
19	YA+ **(TXOE+)**	44	GND
20	GND	45	GND
21	GND	46	GND
22	CK - **(TCLKOUT-)**	47	GND
23	CK+ **(TCLKOUT+)**	48	GND
24	GND	49	GND
25	GND	50	GND

BOM (Bill of Materials) Transmitter PCB:

DS90C3201 Apps TX Demo Board Revision: 0c
Bill Of Materials February 18,2005 17:00:16

Item	Qty	Reference	Part	PCB Footprint
1	2	C1,C2	2.2uF	CAP/EIA-B
2	3	C3,C5,C40	0.1uF	CAP/HDC-1206
3	14	C4,C6,C7,C8,C9,C12,C21, C22,C25,C28,C29,C38,C39, C42	22uF	CAP/EIA-D
4	11	C10,C13,C16,C18,C19,C23, C26,C30,C34,C36,C37	0.1uF	CAP/HDC-0603
5	11	C11,C14,C15,C17,C20,C24, C27,C31,C32,C33,C35	0.01uF	CAP/HDC-0603
6	1	C41	0.01uF	CAP/HDC-0805
7	2	F1,F2	32VDC1A	Fuse/0603 (1608)
8	1	JP74	2-Pin Header	Header/2P
8a	1	JP1-JP21,	21X2-Pin Header	Header/42P
8b	1	JP22-JP49,	28X2-Pin Header	Header/56P
8c	1	JP50-JP71	22X2-Pin Header	Header/44P
9	4	JP72,JP73,JP77,JP78	3 pin Jumper	JUMP/3P
10	2	JP76,JP75	IDC2X2_Unshrouded	CON/HDR-4P-A
11	1	JP79	HEADER 4x1	HDR/4P
12	1	JP80	3 pin Jumper OPEN	JUMP/3P
13	1	J1	IDC25X2_Shrouded	IDC-50
14	4	J2,J3,J4,J5	BANANA	CON/BANANA-S
15	1	J6	DIP 4X2	DIP-8
16	11	L1,L2,L3,L4,L5,L6,L7,L8, L9,L10,L11	Z = 90 ohm	20mm x 12mm
17	70	R1,R2,R3,R4,R5,R6,R7,R8, R9,R10,R11,R12,R13,R14,	49.9ohmOPEN	RES/HDC-0201

		R15,R16,R17,R18,R19,R20, R21,R22,R23,R24,R25,R26, R27,R28,R29,R30,R31,R32, R33,R34,R35,R36,R37,R38, R39,R40,R41,R42,R43,R44, R45,R46,R47,R48,R49,R50, R51,R52,R53,R54,R55,R56, R57,R58,R59,R60,R61,R62, R63,R64,R65,R66,R67,R68, R69,R70		
18	1	R71	49.9ohmOPEN	RES/HDC-0805
19	1	R72	10K OPEN	RES/HDC-0805
20	1	R73	0 Ohm,0805 OPEN	RES/HDC-0805
21	11	R74,R75,R76,R77,R78,R79, R80,R81,R82,R83,R84	100ohm,0805	RES/HDC-0805
22	11	R85,R86,R87,R88,R89,R90, R91,R92,R95,R96,R97	0 Ohm,0402	RES/HDC-0402
23	8	R93,R94,R98,R99,R100, R101,R102,R103	4.75K	RES/HDC-0805
24	7	R104,R105,R106,R107,R108, R109,R110	10K	RES/HDC-0805
25	1	S1	SW DIP-4	DIP-8
26	1	S2	SW DIP-3	DIP-6
27	1	U1	DS90C3201	128ldTQFP_VJX128A

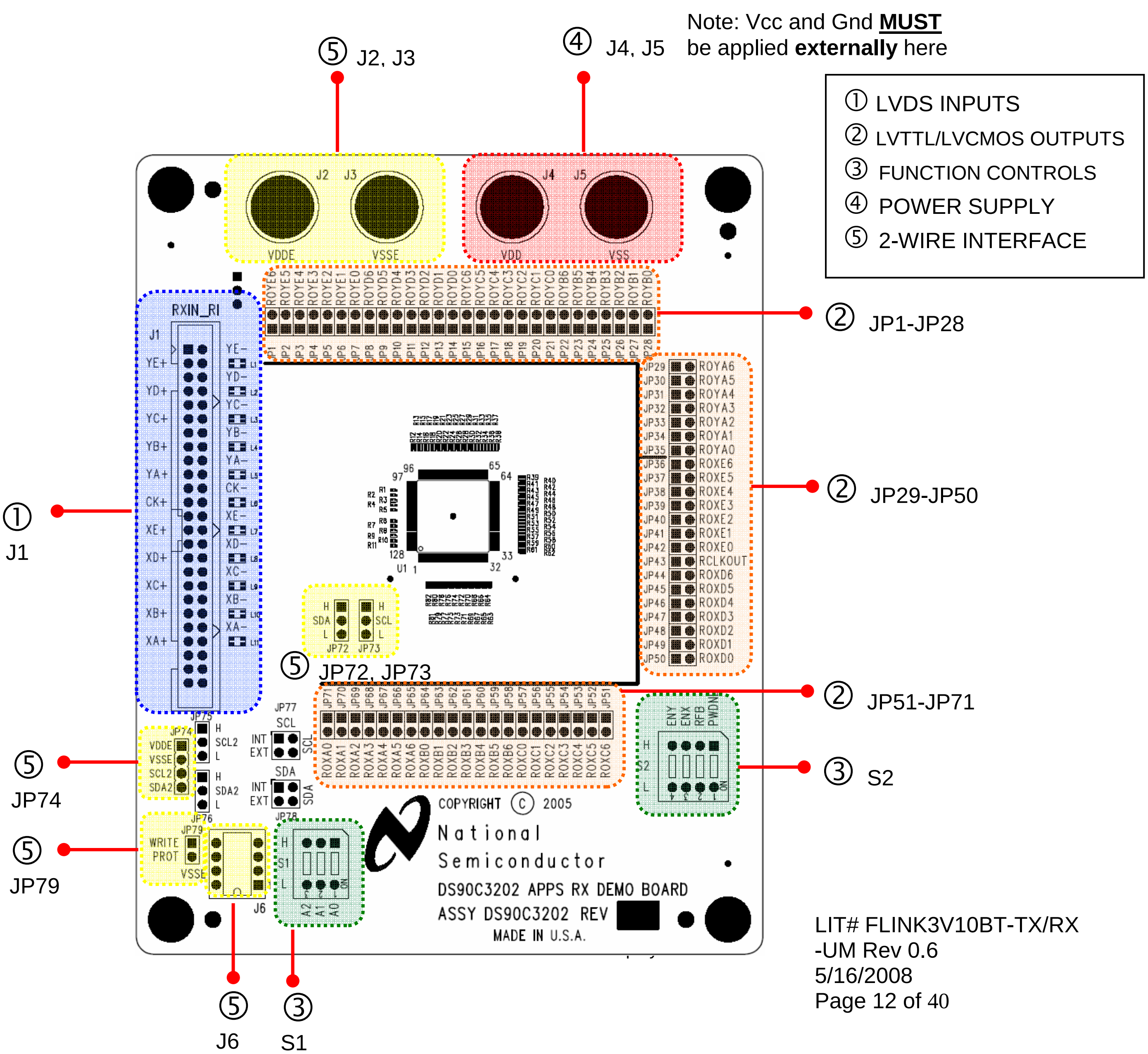
Rx FPD-Link Receiver Board:

Reference JP1 to JP71 provides access to the 70 bit LVTTL/LVCMOS and clock outputs.

The FPD-Link Receiver board is powered externally from the J4 and J5 connectors shown below. For the receiver to be operational, the Power Down (PWDN) switch on S2 must be set. Rising or falling edge reference clock is also selected by S2 tied to HIGH (rising) or LOW (falling). Other device features and configurations can be programmed via 2-wire serial interface interface through J74.

The 50-pin IDC connector (J1) provides the interface for LVDS signals for the Receiver board.

TDK EMC common-mode filters have been added in series on the LVDS signals for high-frequency noise suppression.

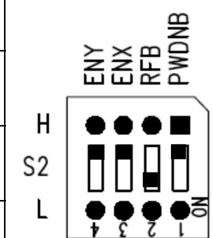


Configuration Settings for the Rx Board

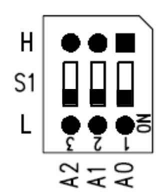
Reference	Description	Open	Closed
WRITE PORT (J79)	2-wire Serial Interface Write Protect	Write Enabled	Write-Protected

Default setting for J79 is set Open (to VSS), Write Enabled.

S2: Receiver Features Selection

Reference	Description	L	H	S2
ENY ***(MODE1)***	**EN**able "**Y**" Bank *"ODD" Data Channels*	Disabled	Enabled (Default)	
ENX ***(MODE0)***	**EN**able "**X**" Bank *"EVEN" Data Channels*	Disabled	Enabled (Default)	
RFB	**R**ising or **F**alling Data Strobe	Falling (Default)	Rising	
PWDNB	**P**o**W**er**D**ow**N B**ar	Powers Down	Operational (Default)	

S2: External EEPROM Slave Address

Reference	Description	S1
A2	Slave Address A2 (Default LOW)	
A1	Slave Address A1 (Default LOW)	
A0	Slave Address A0 (Default LOW)	

Default setting for S1 is set to all LOW, External EEPROM Slave Address A[2:0]=000

Rx LVDS Pinout and LVTTL/LVCMOS by IDC Connector

The following two figures illustrate how the Rx outputs are mapped to the IDC connectors JP1 to JP71 (Note – labels are also printed on the demo boards). The LVDS 50-pin IDC connector (J1) pinout is also shown.

LVDS INPUTS (J1)			
ODD Data Channels		EVEN Data Channels	
Pin No.	Symbol REF **(Pin Name)**	Pin No.	Symbol REF **(Pin Name)**
1	GND	26	XE - **(RXEA-)**
2	YE - **(RXOA-)**	27	XE+ **(RXEA+)**
3	YE+ **(RXOA+)**	28	GND
4	GND	29	GND
5	GND	30	XD - **(RXEB-)**
6	YD - **(RXOB-)**	31	XD+ **(RXEB+)**
7	YD+ **(RXOB+)**	32	GND
8	GND	33	GND
9	GND	34	XC - **(RXEC-)**
10	YC - **(RXOC-)**	35	XC+ **(RXEC+)**
11	YC+ **(RXOC+)**	36	GND
12	GND	37	GND
13	GND	38	XB - **(RXED-)**
14	YB - **(RXOD-)**	39	XB+ **(RXED+)**
15	YB+ **(RXOD+)**	40	GND
16	GND	41	GND
17	GND	42	XA - **(RXEA-)**
18	YA - **(RXOE-)**	43	XA+ **(RXEA+)**
19	YA+ **(RXOE+)**	44	GND
20	GND	45	GND
21	GND	46	GND
22	CK - **(RCLKIN-)**	47	GND
23	CK+ **(RCLKIN+)**	48	GND
24	GND	49	GND
25	GND	50	GND

BANK X OUTPUTS		BANK Y OUTPUTS	
EVEN Data Channels		ODD Data Channels	
Pin No.	Symbol REF **(Pin Name)**	Pin No.	Symbol REF **(Pin Name)**
JP71	ROXA0 **(RXEE0)**	JP35	ROYA0 **(RXOE0)**
JP70	ROXA1 **(RXEE1)**	JP34	ROYA1 **(RXOE1)**
JP69	ROXA2 **(RXEE2)**	JP33	ROYA2 **(RXOE2)**
JP68	ROXA3 **(RXEE3)**	JP32	ROYA3 **(RXOE3)**
JP67	ROXA4 **(RXEE4)**	JP31	ROYA4 **(RXOE4)**
JP66	ROXA5 **(RXEE5)**	JP30	ROYA5 **(RXOE5)**
JP65	ROXA6 **(RXEE6)**	JP29	ROYA6 **(RXOE6)**
JP64	ROXB0 **(RXED0)**	JP28	ROYB0 **(RXOD0)**
JP63	ROXB1 **(RXED1)**	JP27	ROYB1 **(RXOD1)**
JP62	ROXB2 **(RXED2)**	JP26	ROYB2 **(RXOD2)**
JP61	ROXB3 **(RXED3)**	JP25	ROYB3 **(RXOD3)**
JP60	ROXB4 **(RXED4)**	JP24	ROYB4 **(RXOD4)**
JP59	ROXB5 **(RXED5)**	JP23	ROYB5 **(RXOD5)**
JP58	ROXB6 **(RXED6)**	JP22	ROYB6 **(RXOD6)**
JP57	ROXC0 **(RXEC0)**	JP21	ROYC0 **(RXOC0)**
JP56	ROXC1 **(RXEC1)**	JP20	ROYC1 **(RXOC1)**
JP55	ROXC2 **(RXEC2)**	JP19	ROYC2 **(RXOC2)**
JP54	ROXC3 **(RXEC3)**	JP18	ROYC3 **(RXOC3)**
JP53	ROXC4 **(RXEC4**)	JP17	ROYC4 **(RXOC4**)
JP52	ROXC5 **(RXEC5)**	JP16	ROYC5 **(RXOC5)**
JP51	ROXC6 **(RXEC6)**	JP15	ROYC6 **(RXOC6)**
JP50	ROXD0 **(RXEB0)**	JP14	ROYD0 **(RXOB0)**
JP49	ROXD1 **(RXEB1)**	JP13	ROYD1 **(RXOB1)**
JP48	ROXD2 **(RXEB2)**	JP12	ROYD2 **(RXOB2)**
JP47	ROXD3 **(RXEB3)**	JP11	ROYD3 **(RXOB3)**
JP46	ROXD4 **(RXEB4)**	JP10	ROYD4 **(RXOB4)**
JP45	ROXD5 **(RXEB5)**	JP9	ROYD5 **(RXOB5)**
JP44	ROXD6 **(RXEB6)**	JP8	ROYD6 **(RXOB6)**
JP42	ROXE0 **(RXEA0)**	JP7	ROYE0 **(RXOA0)**
JP41	ROXE1 **(RXEA1)**	JP6	ROYE1 **(RXOA1)**
JP40	ROXE2 **(RXEA2)**	JP5	ROYE2 **(RXOA2)**
JP39	ROXE3 **(RXEA3)**	JP4	ROYE3 **(RXOA3)**
JP38	ROXE4 **(RXEA4)**	JP3	ROYE4 **(RXOA4)**
JP37	ROXE5 **(RXEA5)**	JP2	ROYE5 **(RXOA5)**
JP36	ROXE6 **(RXEA6)**	JP1	ROYE6 **(RXOA6)**
JP43		RCLKOUT **(RCLKOUT)**	

BOM (Bill of Materials) Receiver PCB:

DS90C3202 APPS RX Demo Board Revision: 1
Bill Of Materials February 16,2005 13:19:22

Item	Qty	Reference	Part	PCB Footprint
1	2	C4,C1	2.2uF	CAP/EIA-B
2	3	C2,C5,C108	0.1uF	CAP/HDC-1206
3	13	C3,C6,C35,C36,C41,C42, C47,C52,C55,C62,C63,C64, C110	22uF	CAP/EIA-D
4	71	C7,C8,C9,C10,C11,C12,C13, C14,C15,C16,C17,C18,C19, C20,C21,C22,C23,C24,C25, C26,C27,C28,C29,C30,C31, C32,C33,C34,C65,C66,C67, C68,C69,C70,C71,C72,C73, C74,C75,C76,C77,C78,C79, C80,C81,C82,C83,C84,C85, C86,C87,C88,C89,C90,C91, C92,C93,C94,C95,C96,C97, C98,C99,C100,C101,C102, C103,C104,C105,C106,C107	open0402	CAP/HDC-0402
5	10	C37,C39,C43,C46,C48,C51, C53,C57,C59,C61	0.01uF	CAP/HDC-0603
6	10	C38,C40,C44,C45,C49,C50, C54,C56,C58,C60	0.1uF	CAP/HDC-0603
7	1	C109	0.01uF	CAP/HDC-0805
8	2	F2,F1	32VDC1A	Fuse/0603 (1608)
9	1	JP79	2-Pin Header	Header/2P
9a	1	JP1-JP28,	28X2-Pin Header	Header/56P
9b	1	JP29-JP50,	22X2-Pin Header	Header/44P
9c	1	JP51-JP71	21X2-Pin Header	Header/42P
10	4	JP72,JP73,JP75,JP76	3 pin Jumper	JUMP/3P
11	1	JP74	HEADER 4x1	HDR/4P

12	2	JP78,JP77	IDC2X2_Unshrouded	CON/HDR-4P-A
13	1	JP80	3 pin Jumper OPEN	JUMP/3P
14	1	J1	IDC25X2_Shrouded	IDC-50
15	4	J2,J3,J4,J5	BANANA	CON/BANANA-S
16	1	J6	DIP 4X2	DIP-8
17	11	L1,L2,L3,L4,L5,L6,L7,L8, L9,L10,L11	Z = 90 ohm	20mm x 12mm
18	11	R1,R2,R3,R4,R5,R6,R7,R8, R9,R10,R11	100ohm,0201	RES/HDC-0201
19	71	R12,R13,R14,R15,R16,R17, R18,R19,R20,R21,R22,R23, R24,R25,R26,R27,R28,R29, R30,R31,R32,R33,R34,R35, R36,R37,R38,R39,R40,R41, R42,R43,R44,R45,R46,R47, R48,R49,R50,R51,R52,R53, R54,R55,R56,R57,R58,R59, R60,R61,R62,R63,R64,R65, R66,R67,R68,R69,R70,R71, R72,R73,R74,R75,R76,R77, R78,R79,R80,R81,R82	open,0201	RES/HDC-0201
20	1	R83	10K OPEN	RES/HDC-0805
21	1	R84	0 Ohm,0805 OPEN	RES/HDC-0805
22	10	R85,R86,R87,R88,R89,R90, R91,R92,R95,R96	0 Ohm,0402	RES/HDC-0402
23	8	R93,R94,R97,R98,R103, R104,R105,R106	4.75K	RES/HDC-0805
24	7	R99,R100,R101,R102,R107, R108,R109	10K	RES/HDC-0805
25	1	S1	SW DIP-3	DIP-6
26	1	S2	SW DIP-4	DIP-8
27	1	U1	DS90C3202	128ldTQFP_VJX128A

Typical Connection and Test Equipment

The following is a list of typical test equipment that may be used to generate signals for the TX inputs:

1) Digital Video Source – for generation of specific display timing such as Digital Video Processor or Graphics Controller with digital RGB (LVTTL) output.
2) Astro Systems VG-835 - This video generator may be used for both video signal sources for 10-bit Digital RGB and 10-bit LVDS.
3) Any other signal / video generator that generates the correct input levels as specified in the datasheet.
4) Optional – Logic Analyzer or Oscilloscope

The following is a list of typically test equipment that may be used to monitor the output signals from the RX:

1) LCD Display Panel which supports digital RGB (LVTTL) inputs.
2) Astro Systems VG-835 - This video generator may be used for both video signal sources for 10-bit Digital RGB and 10-bit LVDS.
3) Optional – Logic Analyzer or Oscilloscope
4) Any SCOPE with 50 Ohm inputs or high impedance probes.

LVDS signals may be easily measured with high impedance / high bandwidth differential probes such as the TEK P6247 or P6248 differential probes.

EEPROM Programming:

1) Future Designs, Inc. PC-I2C-KIT – This kit interfaces with IBM PC Compatible and allows bi-directional communications with 2-wire serial interface peripherals.

The picture below shows a typical test set up using a Graphics Controller and LCD Panel.

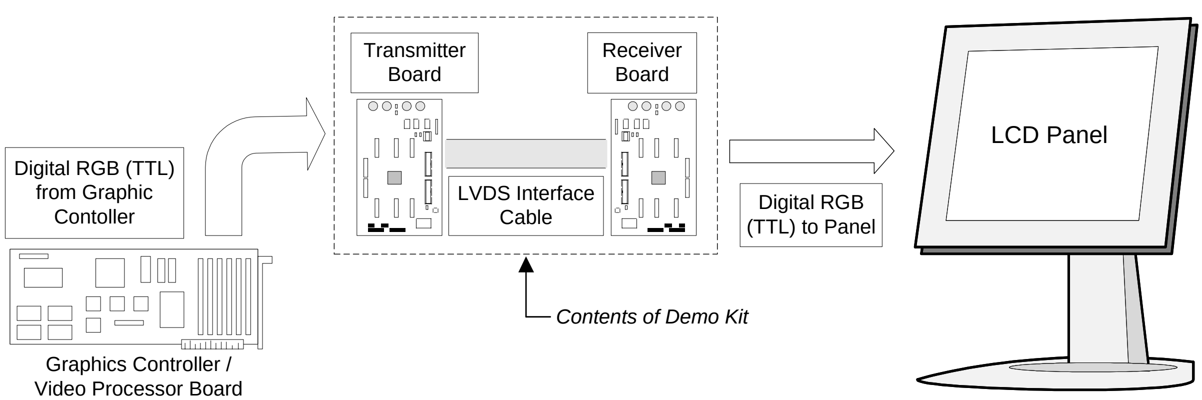


Figure 2. Typical FPD-Link Setup of LCD Panel Application

The picture below shows a typical test set up using a generator and scope.

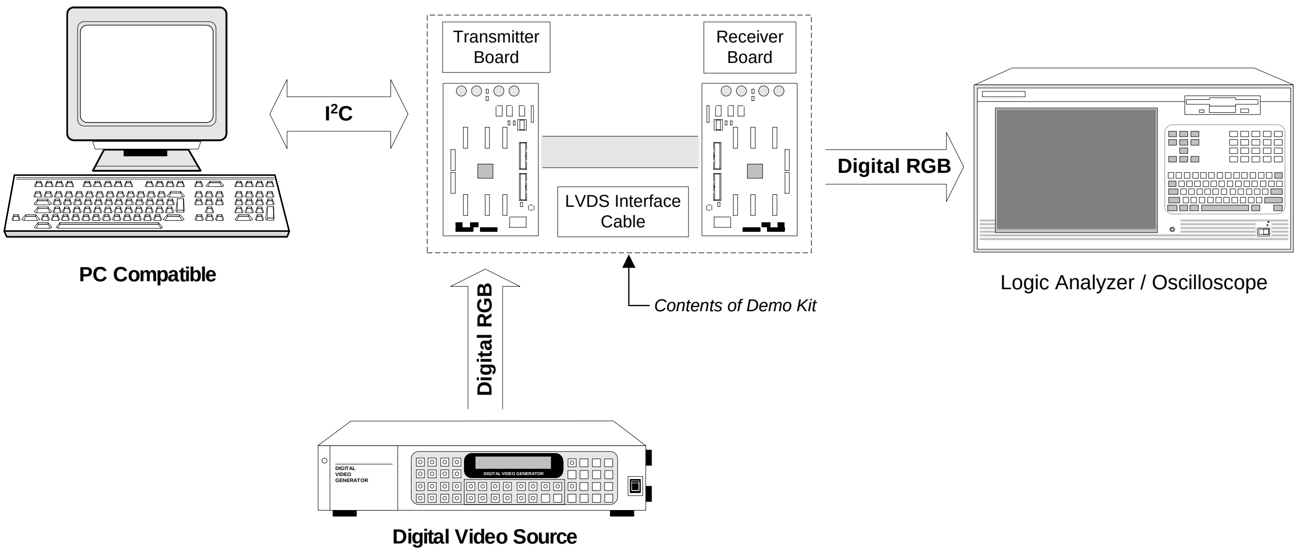


Figure 3. Typical FPD-Link Test Setup for Evaluation

Two-Wire Serial Communication Interface Description

Optional 2-wire serial interface programming allows fine tuning in development and production environments. The DS90C3201/3202 is programmed through a 2-wire serial interface. The 2-wire protocol features a serial clock (S2CLK) and a bi-directional serial data line (S2DATA). The DS90C3201/3202 operates as a slave on the Serial Bus, so the S2CLK line is an input (no clock is generated by the DS90C3201/3202). DS90C3201/3202 has a fixed 7-bit slave address, which is set to 7E'h (1111110'd) and 7C'h (1111100'd) for DS903201/3202 respectively. The PC interface connector JP79 (Tx) and JP74 (Rx) is a 4 pin connector pin header for interfacing with external EEPROM. J79 (Tx) / JP74 (Rx) is designed to interface with the FDI PC-I2C kit through connector or an equivalent type as described. Register values are programmed and stored in an onboard EEPROM via a two wire serial interface and a PC compatible system. Upon power-up, default control register values will be loaded into Tx/Rx. Otherwise, registers may be programmed directly from the EEPROM into the Tx/Rx control registers via this same two wire serial interface method.

LVDS Data Mapping

The FPD-Link Receiver which receives video data and timing through 10 pairs of LVDS channels plus 1 LVDS clock to provide 30-bit dual color depth. The Transmitter converts the LVTTL/LVCMOS parallel lines into ten serialized LVDS data pairs plus a LVDS clock. The video data stream is then converted to LVTTL/LVCMOS parallel data. The device accepts 10-bit / 8-bit / 6-bit single/dual input data mapping as shown and also supports the JEIDA standard for 10-bit LVDS.

	Red		**Green**		**Blue**	
	Single	**Dual**	**Single**	**Dual**	**Single**	**Dual**
10-bit MSB	**R9**	OR9 / ER9	**G9**	OG9 / EG9	**B9**	OB9 / EB9
	R8	OR8 / ER8	**G8**	OG8 / EG8	**B8**	OB8 / EB8
8-bit MSB*	**R7**	OR7 / ER7	**G7**	OG7 / EG7	**B7**	OB7 / EB7
	R6	OR6 / ER6	**G6**	OG6 / EG6	**B6**	OB6 / EB6
6-bit MSB	**R5**	OR5 / ER5	**G5**	OG5 / EG5	**B5**	OB5 / EB5
	R4	OR4 / ER4	**G4**	OG4 / EG4	**B4**	OB4 / EB4
	R3	OR3 / ER3	**G3**	OG3 / EG3	**B3**	OB3 / EB3
	R2	OR2 / ER2	**G2**	OG2 / EG2	**B2**	OB2 / EB2
	R1	OR1 / ER1	**G1**	OG1 / EG1	**B1**	OB1 / EB1
LSB	**R0**	OR0 / ER0	**G0**	OG0 / EG0	**B0**	OB0 / EB0

Note: OR0-OR9, OG0-OG9, OB0-OB9 represents ODD pixel data,
ER0-OR9, EG0-OG9, EB0-OB9 represents EVEN pixel data.

*8-bit conventional color mapping

LVDS Data Mapping (Cont'd)

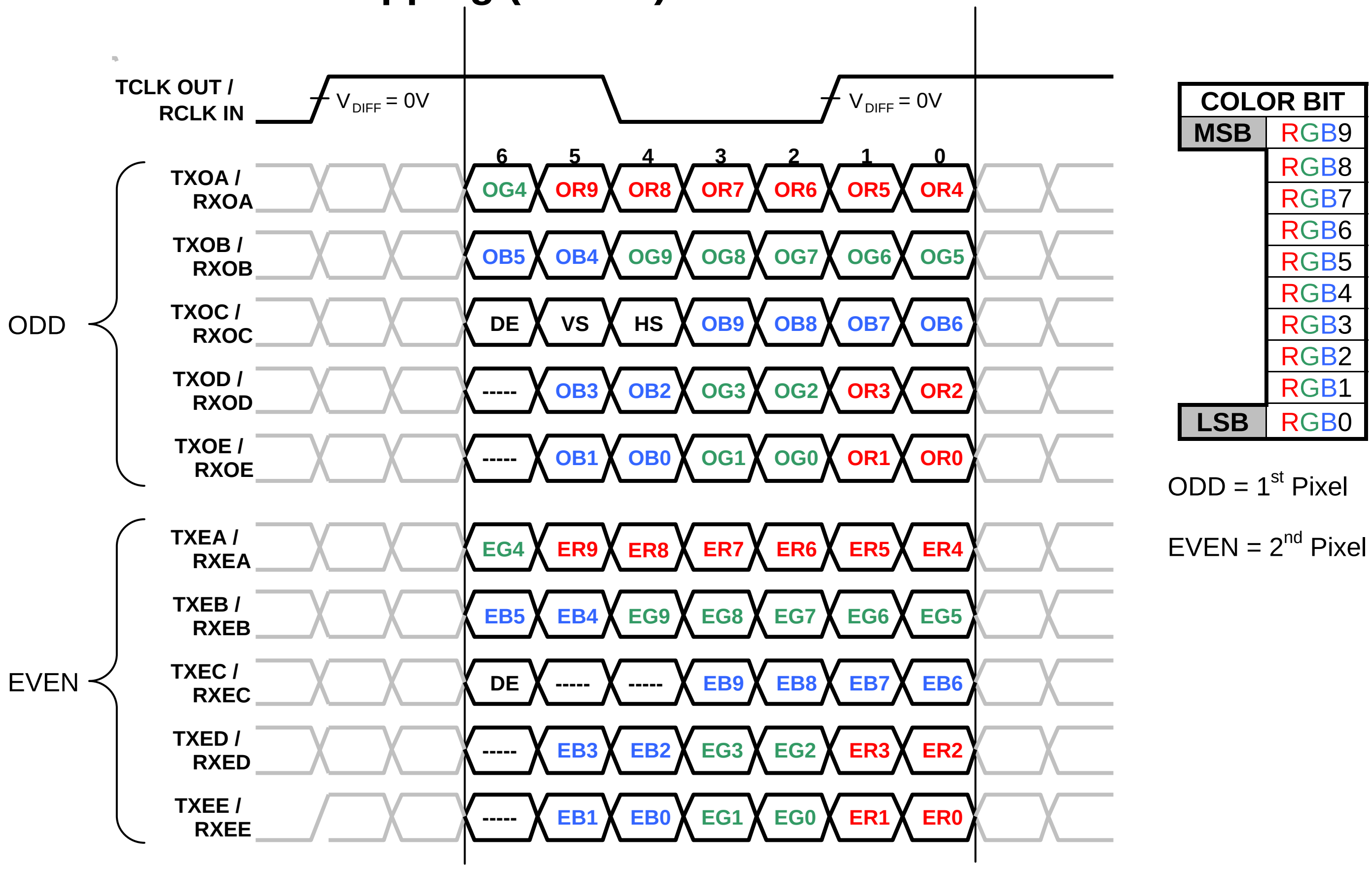


Figure 1. Dual 10-Bit Input Mapping - JEIDA Compatible

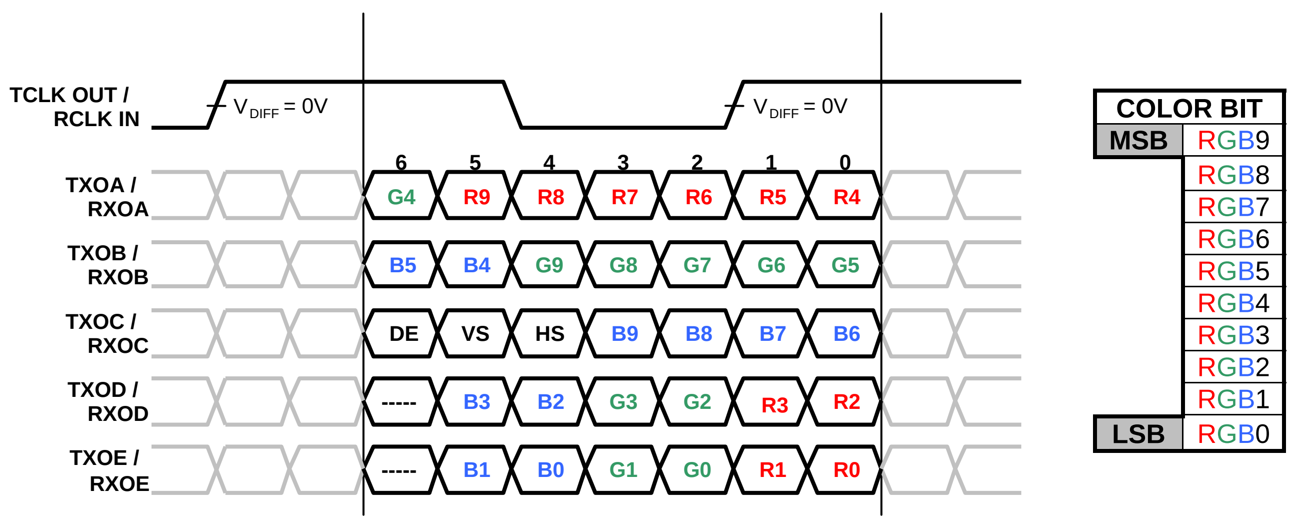


Figure 2. Single 10-Bit Input Mapping - JEIDA Compatible

LVDS Data Mapping (Cont'd)

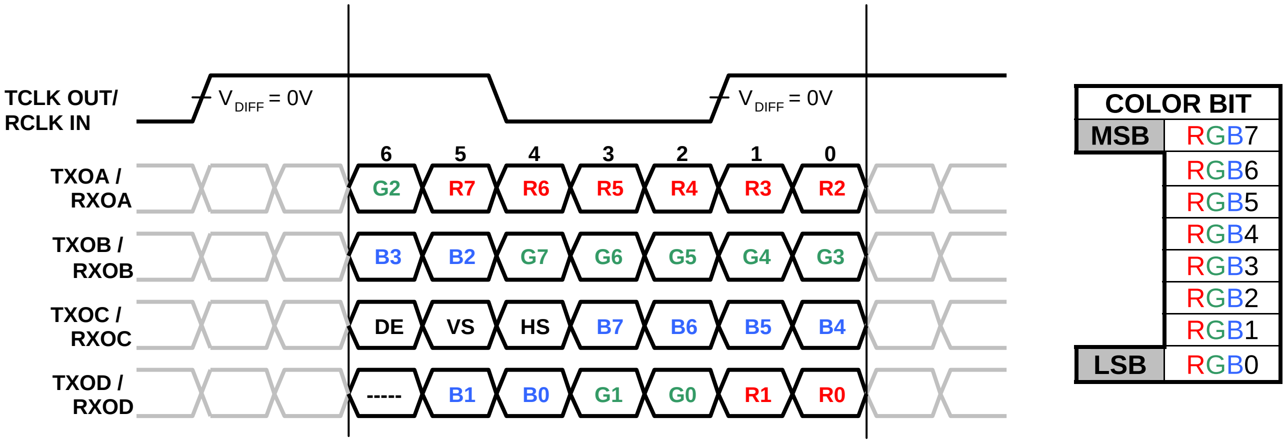


Figure 3a. Single 8-Bit Input Mapping – Conventional Color Mapping

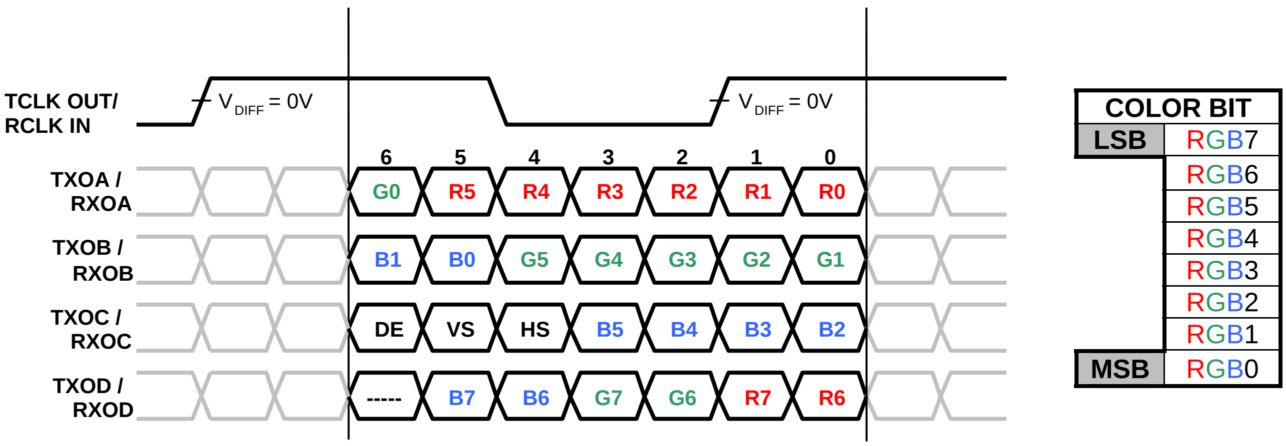


Figure 3b. Single 8-Bit Input Mapping – Alternative Color Mapping

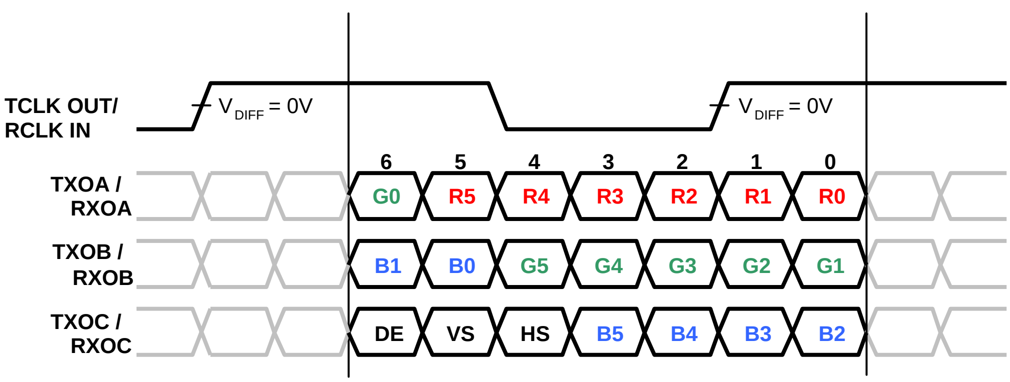
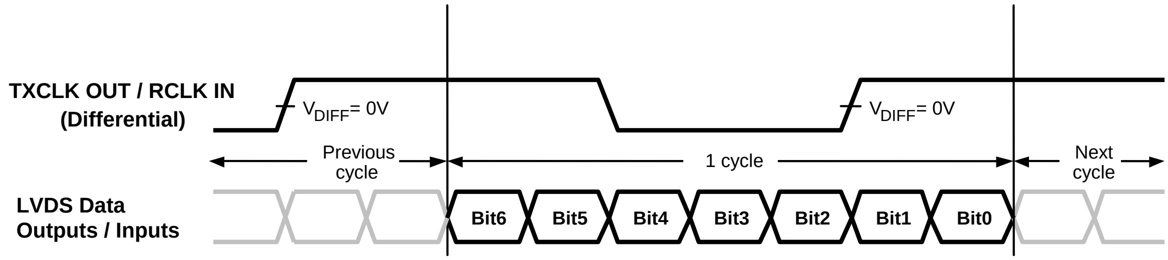


Figure 4. Single 6-Bit Input Mapping

6-bit, 8-bit, 10-bit Application



Single LVDS Data Mapping

LVDS Bit TXO/RXO	1 x 6-bit	1 x 8-bit	1 x 8-bit*	1 x 10-bit
A0	R0	R2	R0	R4
A1	R1	R3	R1	R5
A2	R2	R4	R2	R6
A3	R3	R5	R3	R7
A4	R4	R6	R4	R8
A5	R5	R7	R5	R9
A6	G0	G2	G0	G4
B0	G1	G3	G1	G5
B1	G2	G4	G2	G6
B2	G3	G5	G3	G7
B3	G4	G6	G4	G8
B4	G5	G7	G5	G9
B5	B0	B2	B0	B4
B6	B1	B3	B1	B5
C0	B2	B4	B2	B6
C1	B3	B5	B3	B7
C2	B4	B6	B4	B8
C3	B5	B7	B5	B9
C4	HS	HS	HS	HS
C5	VS	VS	VS	VS
C6	DE	DE	DE	DE
D0		R0	R6	R2
D1		R1	R7	R3
D2		G0	G6	G2
D3		G1	G7	G3
D4		B0	B6	B2
D5		B1	B7	B3
D6		N/A	N/A	N/A
E0				R0
E1				R1
E2				G0
E3				G1
E4				B0
E5				B1
E6				N/A

*Alternative Input Color Mapping

Dual LVDS Data Mapping

LVDS Bit	2 x 6-bit	2 x 8-bit	2 x 8-bit*	2 x 10-bit	LVDS Bit	2 x 6-bit	2 x 8-bit	2 x 8-bit*	2 x 10-bit
TXO/RXO	ODD Pixel Data				TXE/RXE	EVEN Pixel Data			
A0	R0	R2	R0	R4	A0	R0	R2	R0	R4
A1	R1	R3	R1	R5	A1	R1	R3	R1	R5
A2	R2	R4	R2	R6	A2	R2	R4	R2	R6
A3	R3	R5	R3	R7	A3	R3	R5	R3	R7
A4	R4	R6	R4	R8	A4	R4	R6	R4	R8
A5	R5	R7	R5	R9	A5	R5	R7	R5	R9
A6	G0	G2	G0	G4	A6	G0	G2	G0	G4
B0	G1	G3	G1	G5	B0	G1	G3	G1	G5
B1	G2	G4	G2	G6	B1	G2	G4	G2	G6
B2	G3	G5	G3	G7	B2	G3	G5	G3	G7
B3	G4	G6	G4	G8	B3	G4	G6	G4	G8
B4	G5	G7	G5	G9	B4	G5	G7	G5	G9
B5	B0	B2	B0	B4	B5	B0	B2	B0	B4
B6	B1	B3	B1	B5	B6	B1	B3	B1	B5
C0	B2	B4	B2	B6	C0	B2	B4	B2	B6
C1	B3	B5	B3	B7	C1	B3	B5	B3	B7
C2	B4	B6	B4	B8	C2	B4	B6	B4	B8
C3	B5	B7	B5	B9	C3	B5	B7	B5	B9
C4	HS	HS	HS	HS	C4	HS	HS	HS	HS
C5	VS	VS	VS	VS	C5	VS	VS	VS	VS
C6	DE	DE	DE	DE	C6	DE	DE	DE	DE
D0		R0	R6	R2	D0		R0	R6	R2
D1		R1	R7	R3	D1		R1	R7	R3
D2		G0	G6	G2	D2		G0	G6	G2
D3		G1	G7	G3	D3		G1	G7	G3
D4		B0	B6	B2	D4		B0	B6	B2
D5		B1	B7	B3	D5		B1	B7	B3
D6		N/A	N/A	N/A	D6		N/A	N/A	N/A
E0				R0	E0				R0
E1				R1	E1				R1
E2				G0	E2				G0
E3				G1	E3				G1
E4				B0	E4				B0
E5				B1	E5				B1
E6				N/A	E6				N/A

*Alternative Input Color Mapping

Troubleshooting

If the demo boards are not performing properly, use the following as a guide for quick solutions to potential problems. If the problem persists, please contact the local Sales Representative for assistance.

QUICK CHECKS:

1. Check that Power and Ground are connected to both Tx AND Rx boards.
2. Check the supply voltage (typical 3.3V) and also current draw with both Tx and Rx boards (should be about 100mA with clock and one data bit at 135MHz).
3. Verify input clock and input data signals meet requirements (VIL, VIH, tset, thold), Also verify that data is strobed on the selected rising/falling (RFB pin) edge of the clock.
4. Check that the Jumpers and Switches are set correctly.
5. Check that the cable is properly connected.

TROUBLESHOOTING CHART

Problem…	**Solution…**
There is only the output clock. There is no output data.	Make sure the data is applied to the correct input pin. Make sure data is valid at the input.
No output data and clock.	Make sure Power is on. Input data and clock are active and connected correctly. Make sure that the cable is secured to both demo boards.
Power, ground, input data and input clock are connected correctly, but no outputs.	Check the Power Down pins of both boards and make sure that the devices are enabled (/PD=Vcc) for operation.
The devices are pulling more than 1A of current.	Check for shorts in the cables connecting the TX and RX boards.
After powering up the demo boards, the power supply reads less than 3V when it is set to 3.3V.	Use a larger power supply that will provide enough current for the demo boards, a 500mA power supply is recommended.

Additional Information

For more information on FPD-Link Transmitters/Receivers, refer to the National's LVDS website at:

www.national.com/appinfo/fpd

Equipment References

Note: Please note that the following references are supplied only as a courtesy to our valued customers. It is not intended to be an endorsement of any particular equipment supplier.

Digital Video Pattern Generator – Astro Systems VG-835 (or equivalent):

Astro Systems
425 S. Victory Blvd. Suite A
Burbank, CA 91502
Phone: (818) 848-7722
Fax: (818) 848-7799
www.astro-systems.com

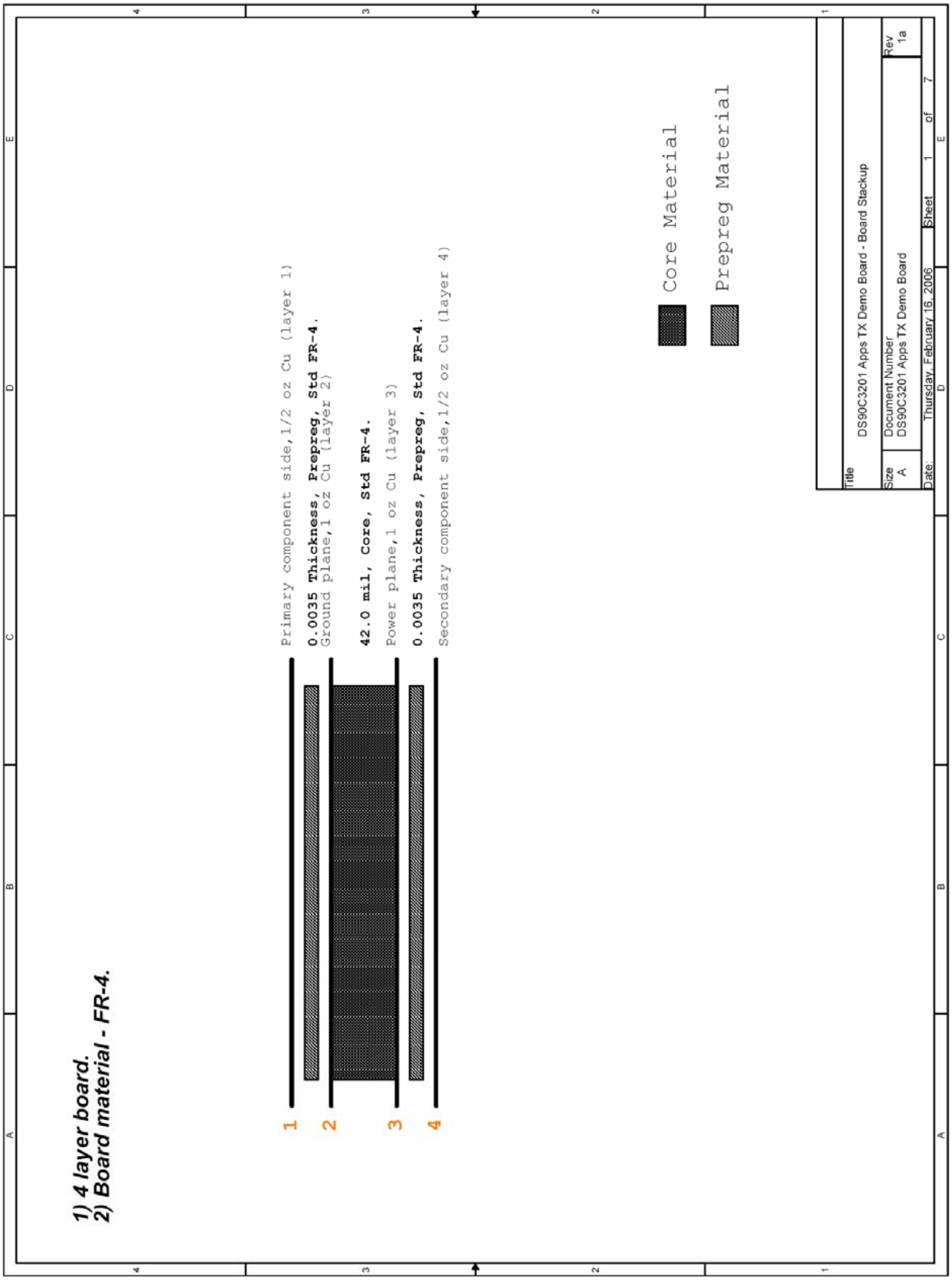
EEPROM Programming – FDI PC-I2C kit (or equivalent):

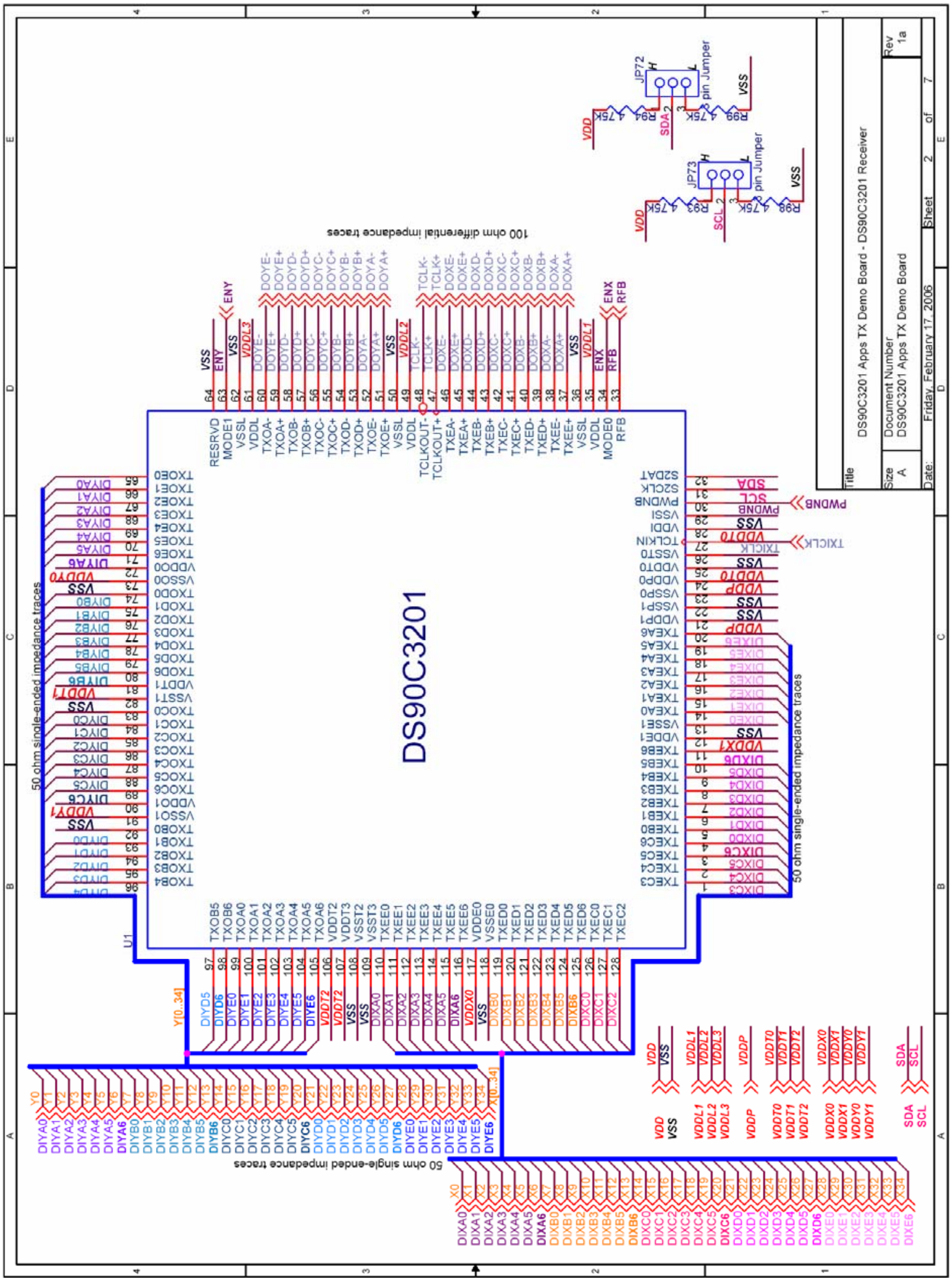
Future Designs, Inc.
2702 Triana Boulevard SW
Huntsville, AL 35805
Sales: (800) 278-0293
Information: (256) 883-1240
FAX: (256) 883-1241
www.teamfdi.com

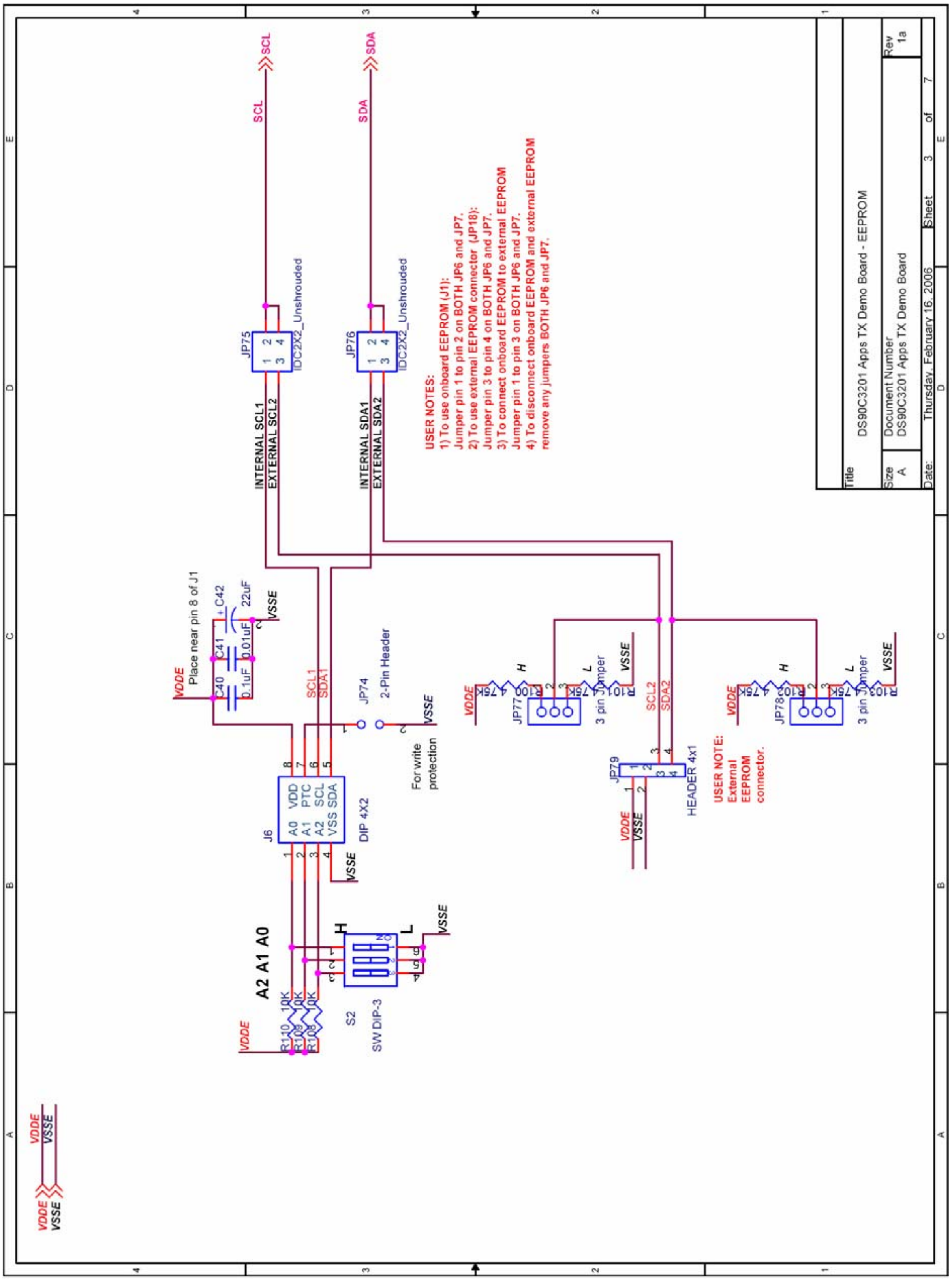
Optional EMI Filters – TDK Chip Beads (or equivalent)
TDK Corporation of America
1740 Technology Drive, Suite 510
San Jose, CA 95110
Phone: (408) 437-9585
Fax: (408) 437-9591
www.component.tdk.com
Local U.S.A. direct contact:
Kazuhiko (Kevin) Umeda
Phone: (408) 467-5222
Email: kumeda@tdktca.com

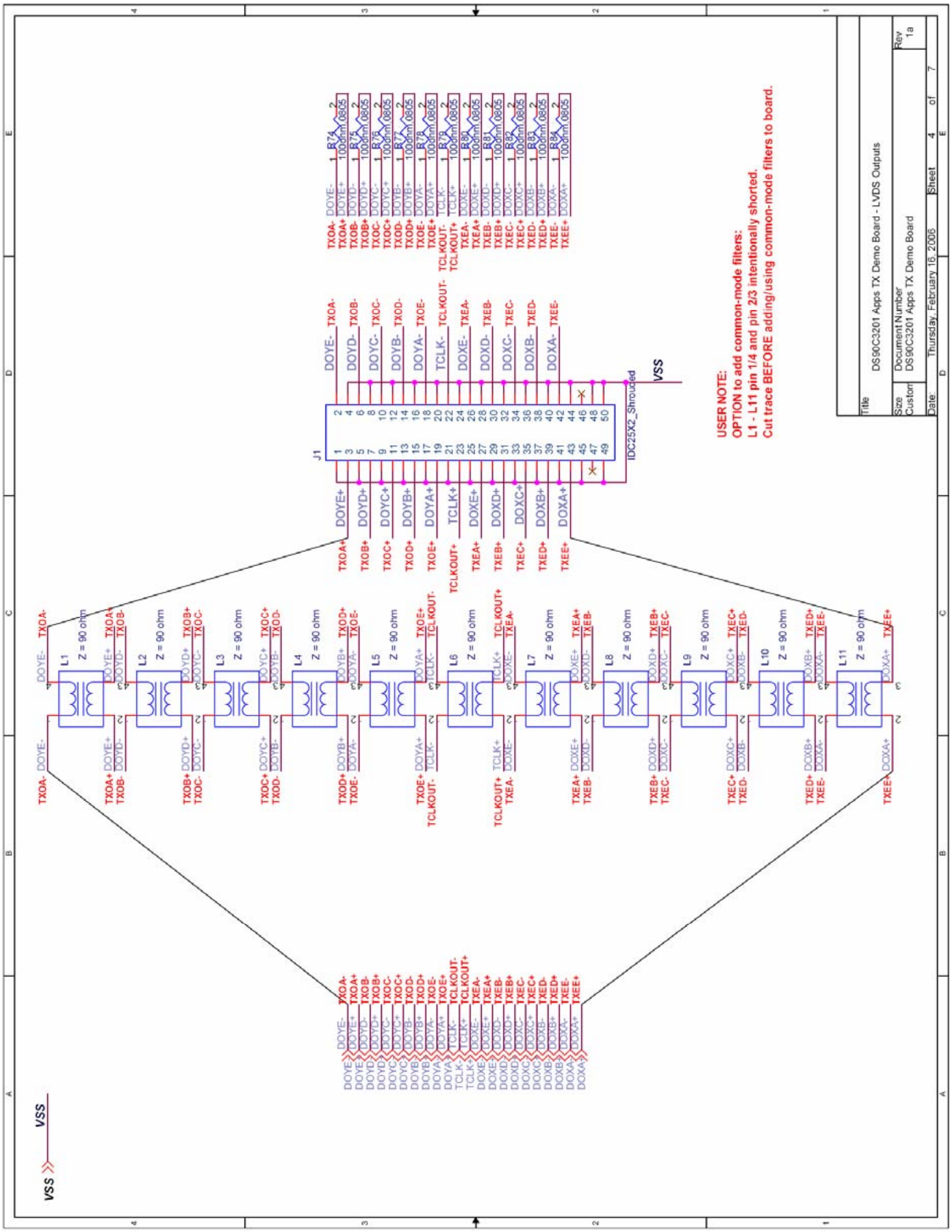
Appendix

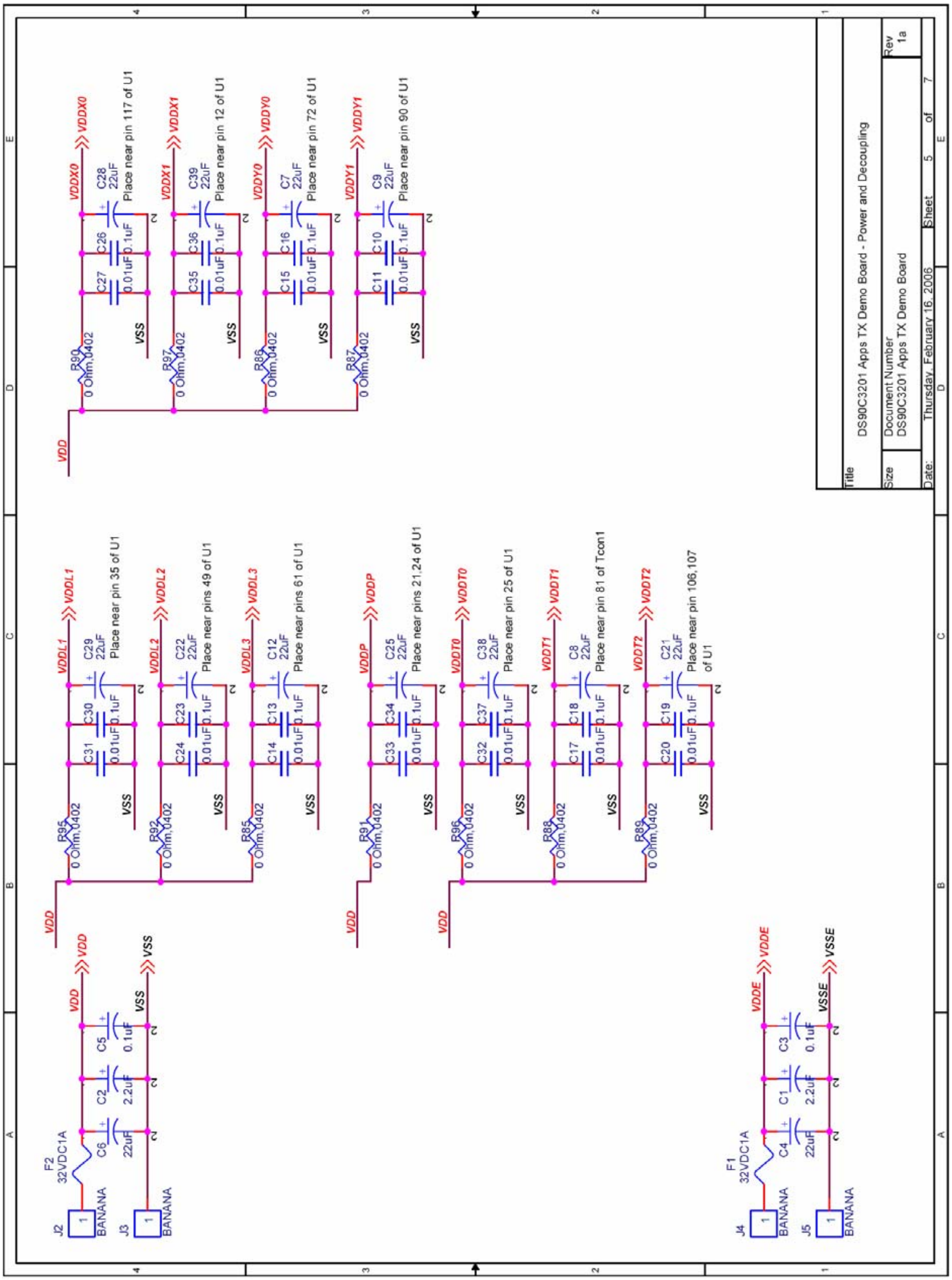
Tx PCB Schematic:

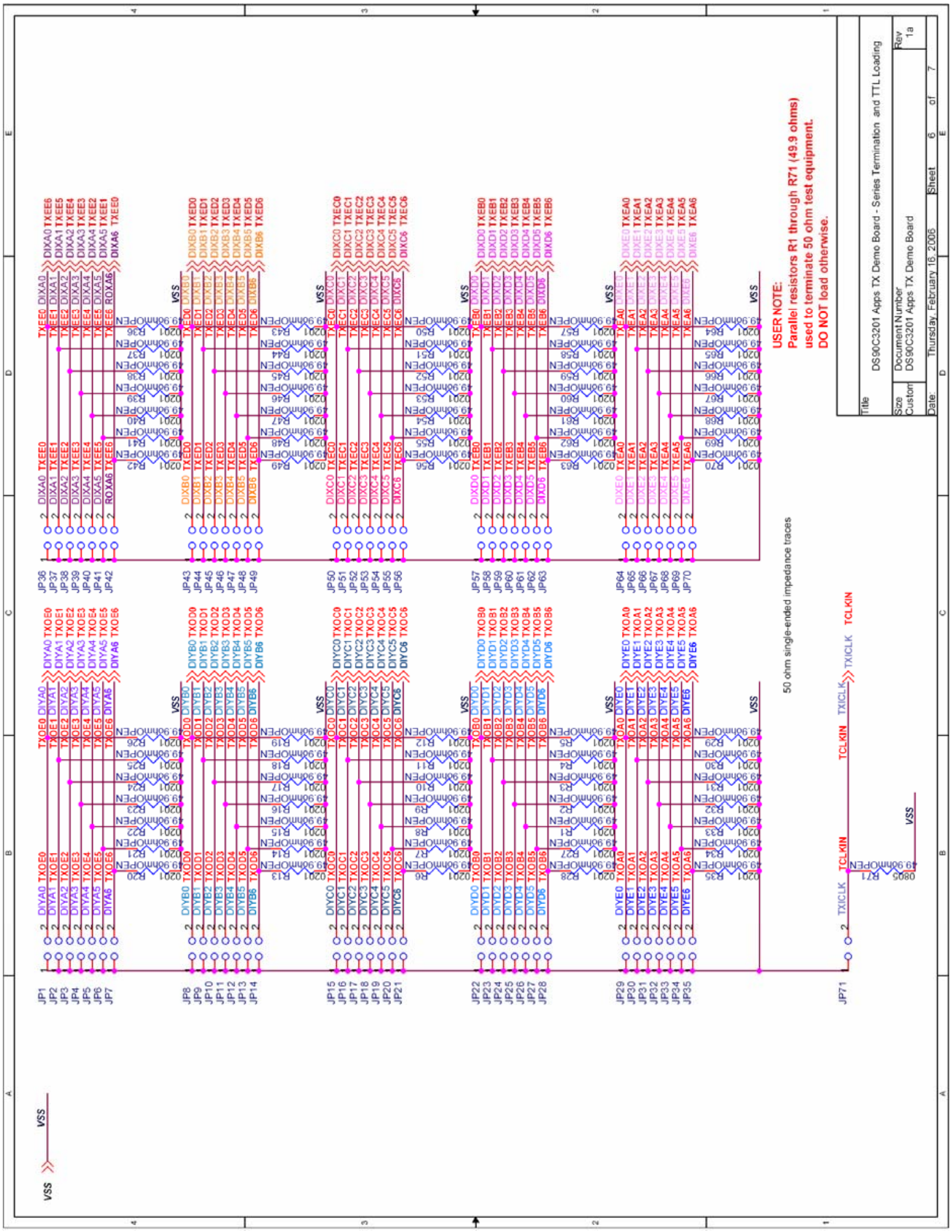


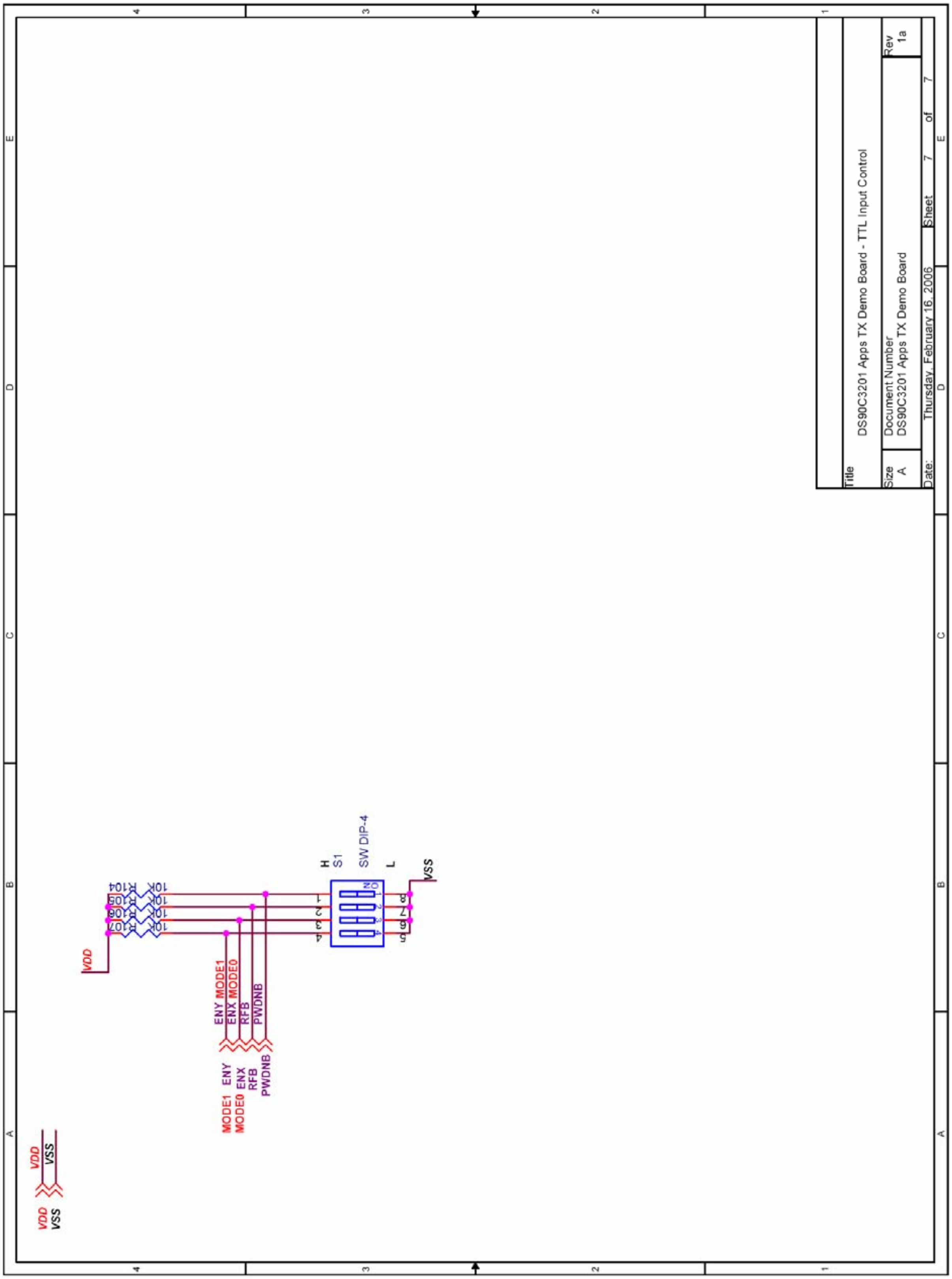

DS90C3201
100 ohm differential impedance traces
50 ohm single-ended impedance traces
Title
DS90C3201 Apps TX Demo Board - DS90C3201 Receiver
Size A
Document Number
DS90C3201 Apps TX Demo Board
Rev 1a
Date: Friday, February 17, 2006
Sheet 2 of 7


USER NOTES:
1) To use onboard EEPROM (J1):
Jumper pin 1 to pin 2 on BOTH JP6 and JP7.
2) To use external EEPROM connector (JP18):
Jumper pin 3 to pin 4 on BOTH JP6 and JP7.
3) To connect onboard EEPROM to external EEPROM
Jumper pin 1 to pin 3 on BOTH JP6 and JP7.
4) To disconnect onboard EEPROM and external EEPROM
remove any jumpers BOTH JP6 and JP7.
USER NOTE:
External
EEPROM
connector.
Place near pin 8 of J1
For write
protection
A2 A1 A0
Title
DS90C3201 Apps TX Demo Board - EEPROM
Size
A
Document Number
DS90C3201 Apps TX Demo Board
Rev
1a
Date: Thursday, February 16, 2006
Sheet 3 of 7

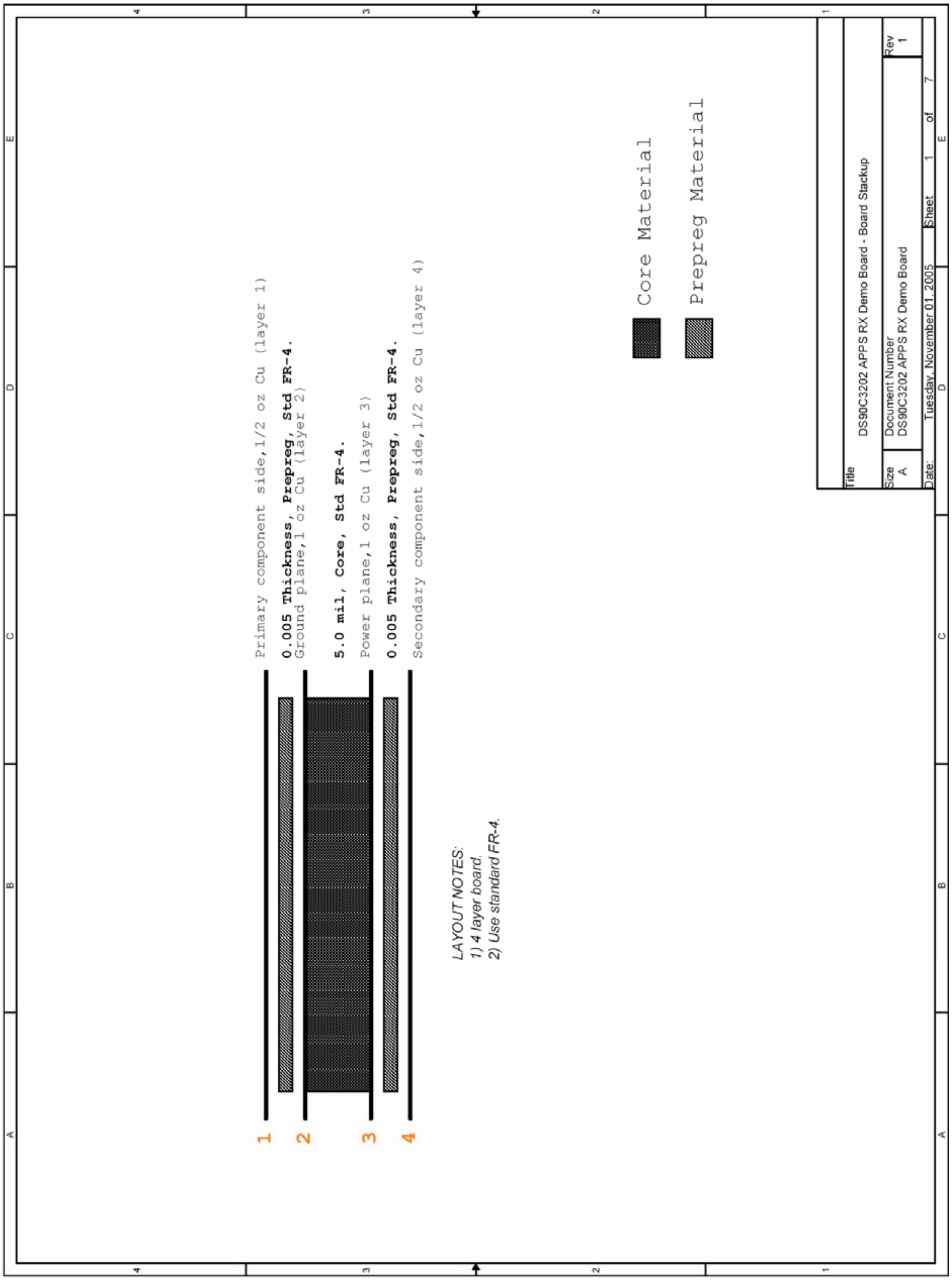

USER NOTE:
OPTION to add common-mode filters:
L1 - L11 pin 1/4 and pin 2/3 intentionally shorted.
Cut trace BEFORE adding/using common-mode filters to board.
VSS
IDC25X2_Shrouded
Title
DS90C3201 Apps TX Demo Board - LVDS Outputs
Size
Custom
Document Number
DS90C3201 Apps TX Demo Board
Rev
1a
Date: Thursday, February 16, 2006
Sheet 4 of 7

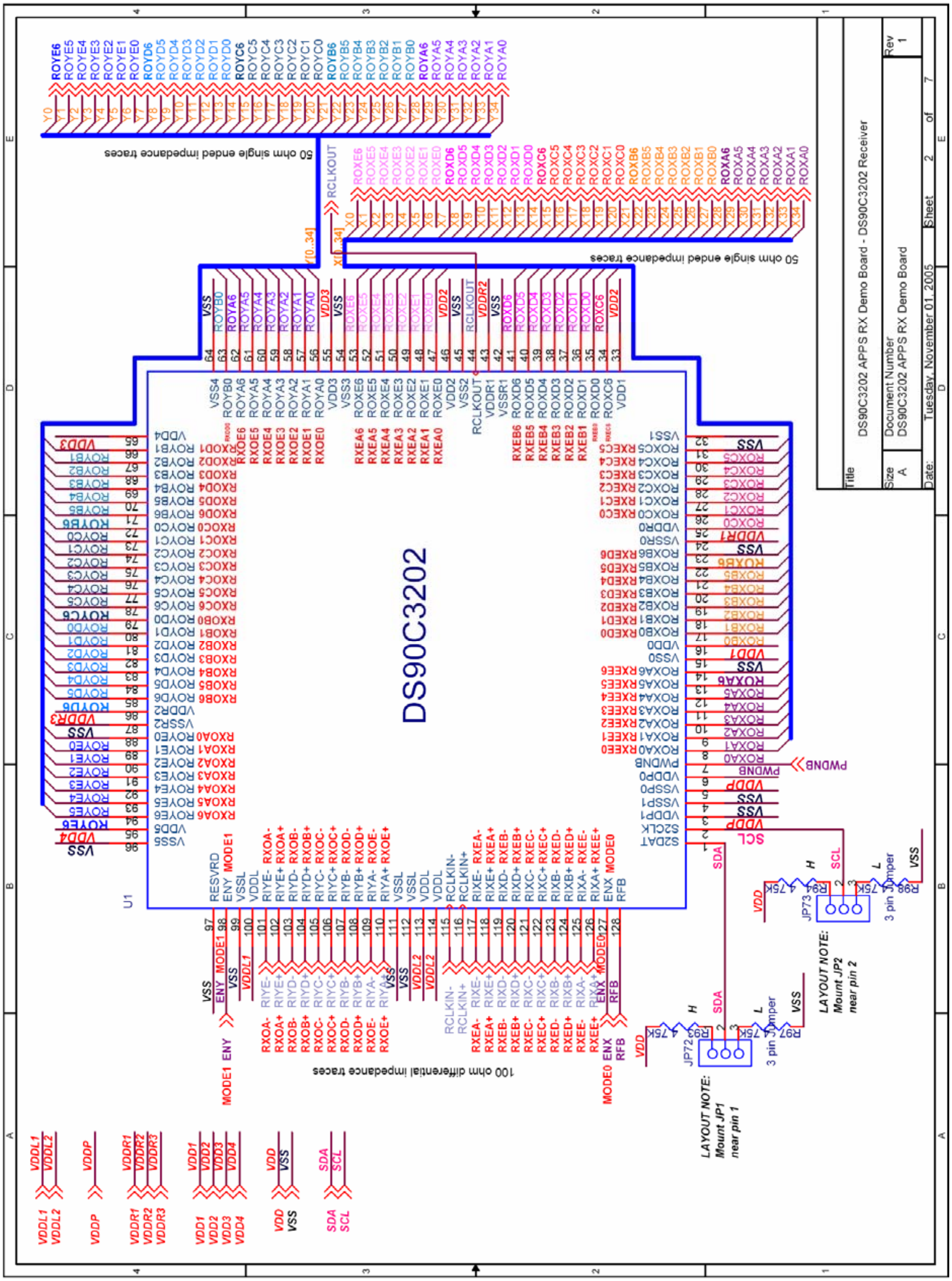

VDDX0
C28
22uF
Place near pin 117 of U1
VDDX1
C39
22uF
Place near pin 12 of U1
VDDY0
C7
22uF
Place near pin 72 of U1
VDDY1
C9
22uF
Place near pin 90 of U1
VDDL1
C29
22uF
Place near pin 35 of U1
VDDL2
C22
22uF
Place near pins 49 of U1
VDDL3
C12
22uF
Place near pins 61 of U1
VDDP
C25
22uF
Place near pins 21,24 of U1
VDDT0
C38
22uF
Place near pin 25 of U1
VDDT1
C8
22uF
Place near pin 81 of Tcon1
VDDT2
C21
22uF
Place near pin 106,107 of U1
VDD
VSS
VDDE
VSSE
0 Ohm,0402
0.1uF
0.01uF
2.2uF
F2
32VDC1A
F1
32VDC1A
BANANA
J2
J3
J4
J5
Title
DS90C3201 Apps TX Demo Board - Power and Decoupling
Size
Document Number
DS90C3201 Apps TX Demo Board
Rev
1a
Date: Thursday, February 16, 2006
Sheet 5 of 7

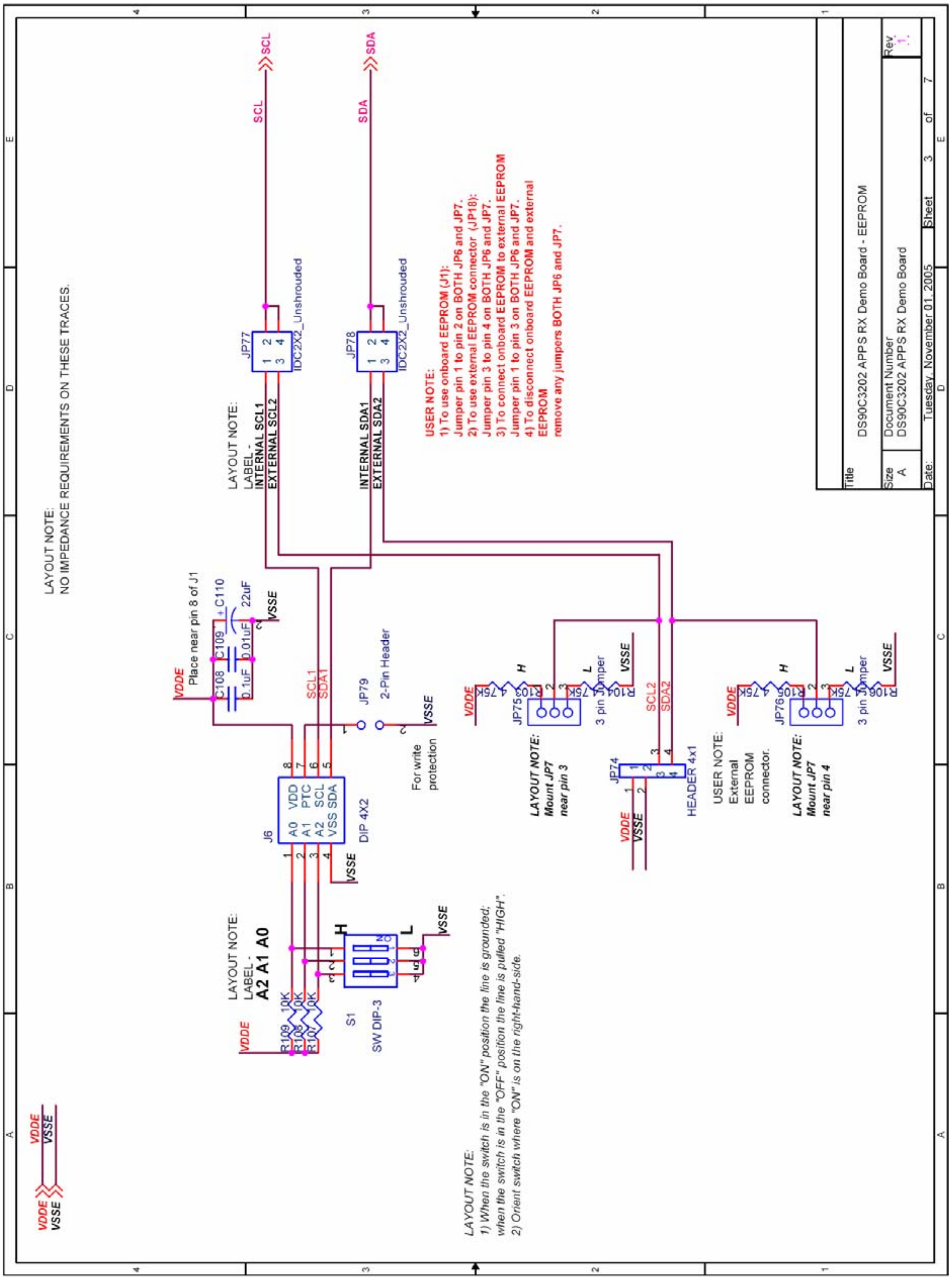

USER NOTE:
Parallel resistors R1 through R71 (49.9 ohms)
used to terminate 50 ohm test equipment.
DO NOT load otherwise.
50 ohm single-ended impedance traces
DS90C3201 Apps TX Demo Board - Series Termination and TTL Loading
DS90C3201 Apps TX Demo Board

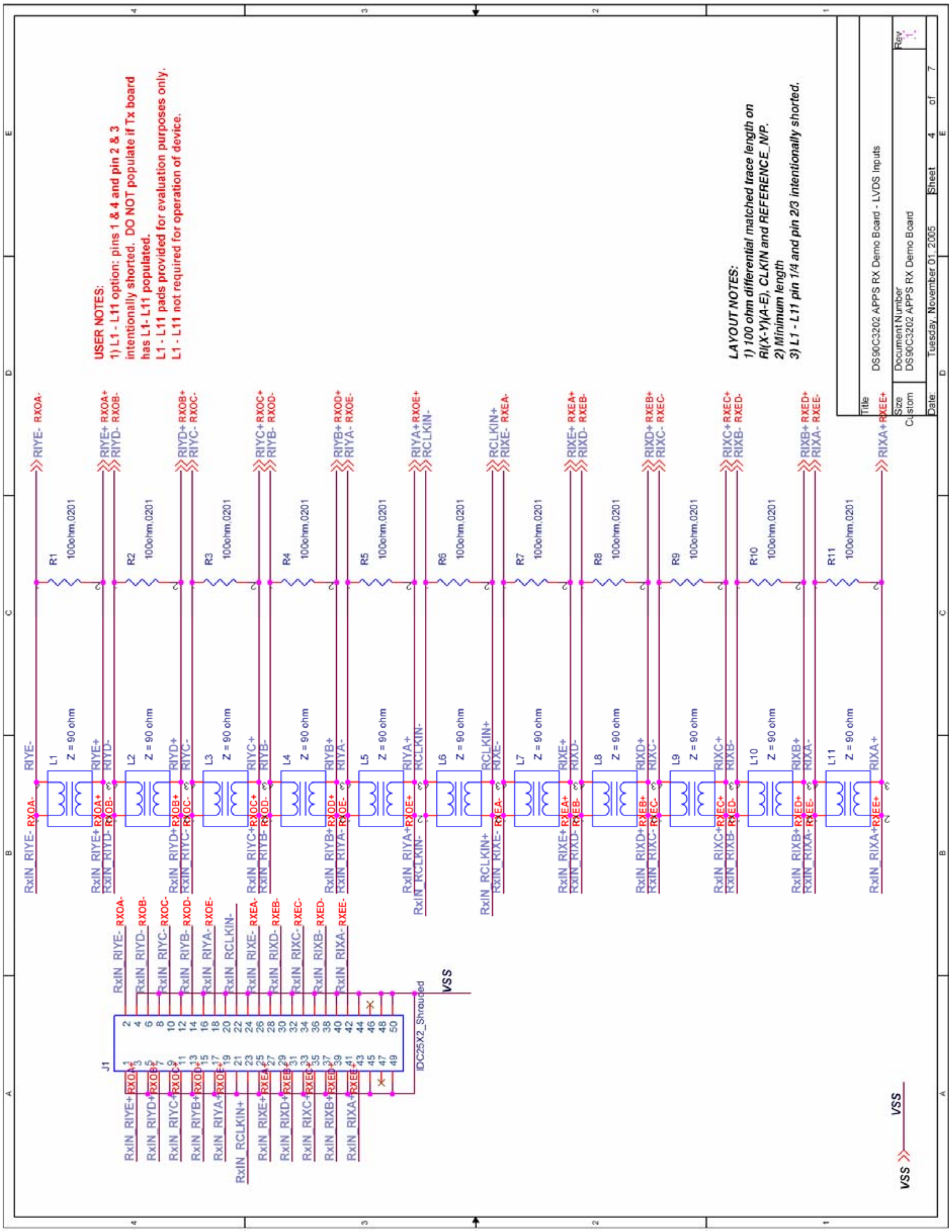

Title
DS90C3201 Apps TX Demo Board - TTL Input Control
Size
A
Document Number
DS90C3201 Apps TX Demo Board
Rev
1a
Date: Thursday, February 16, 2006
Sheet 7 of 7
H
S1
SW DIP-4
L
VSS
VDD
R104
R105
R106
R107
10K
ENY MODE1
ENX MODE0
RFB
PWDNB
MODE1 ENY
MODE0 ENX
RFB
PWDNB
VDD
VSS

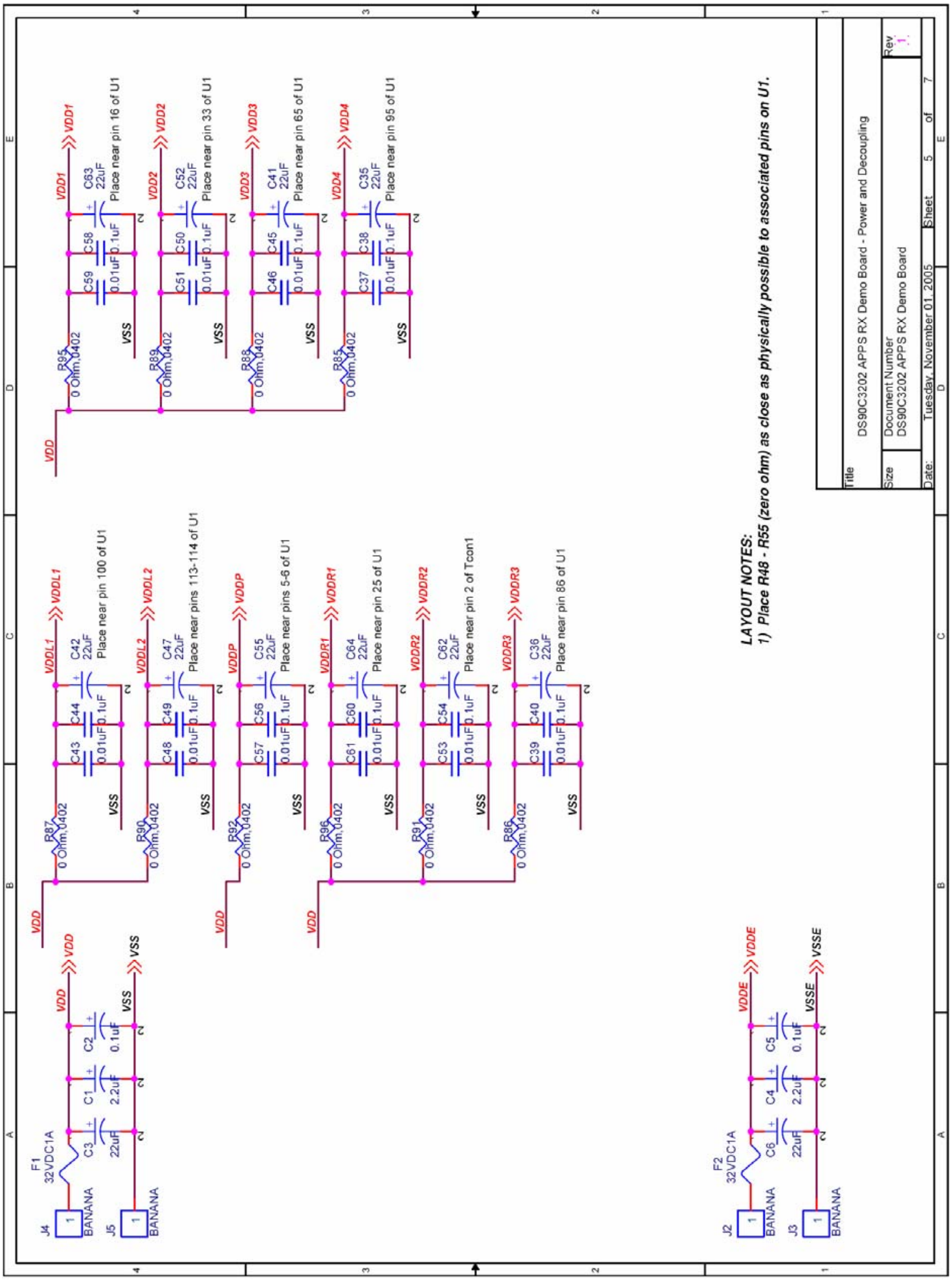
Rx PCB Schematic:

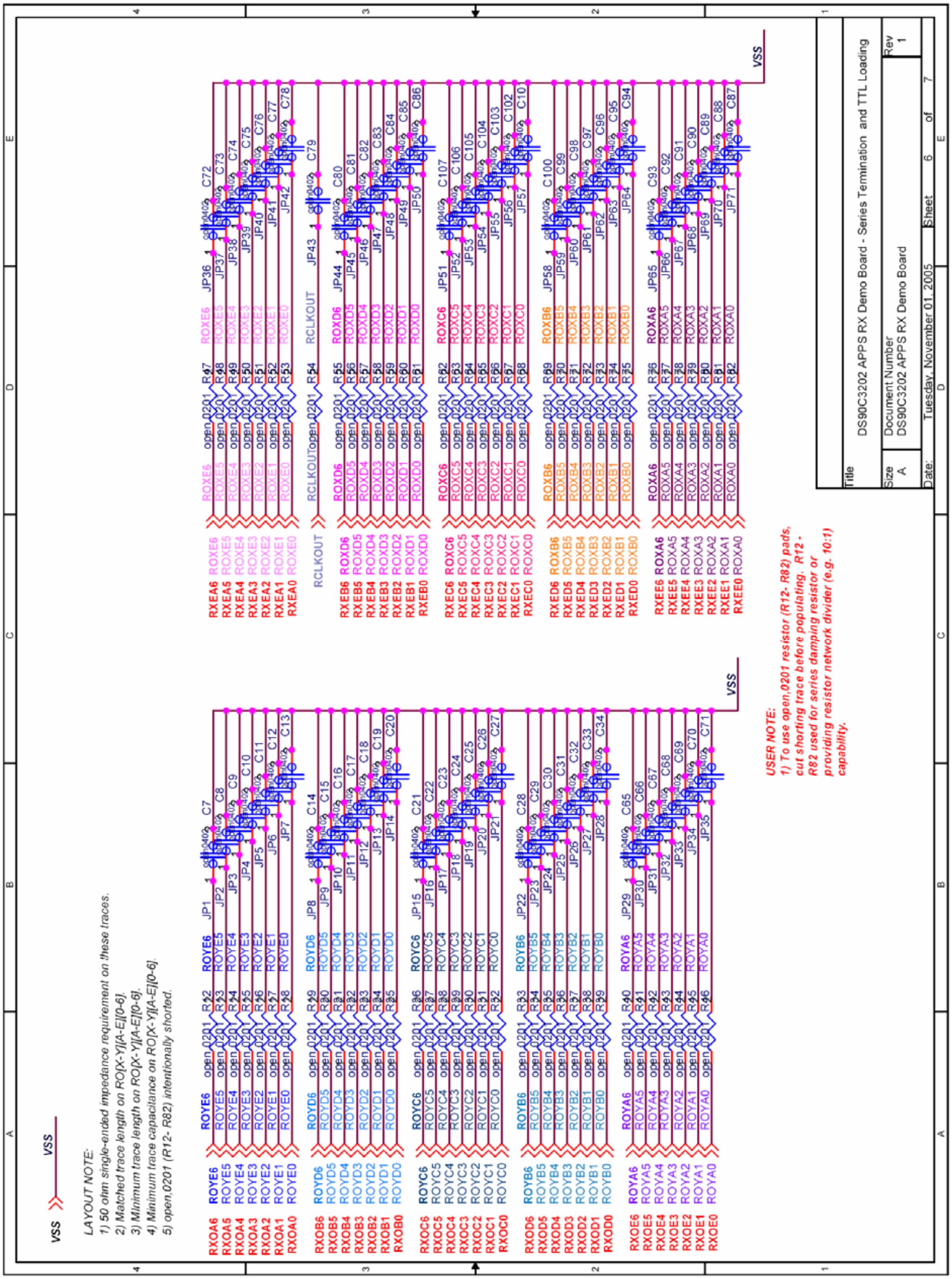


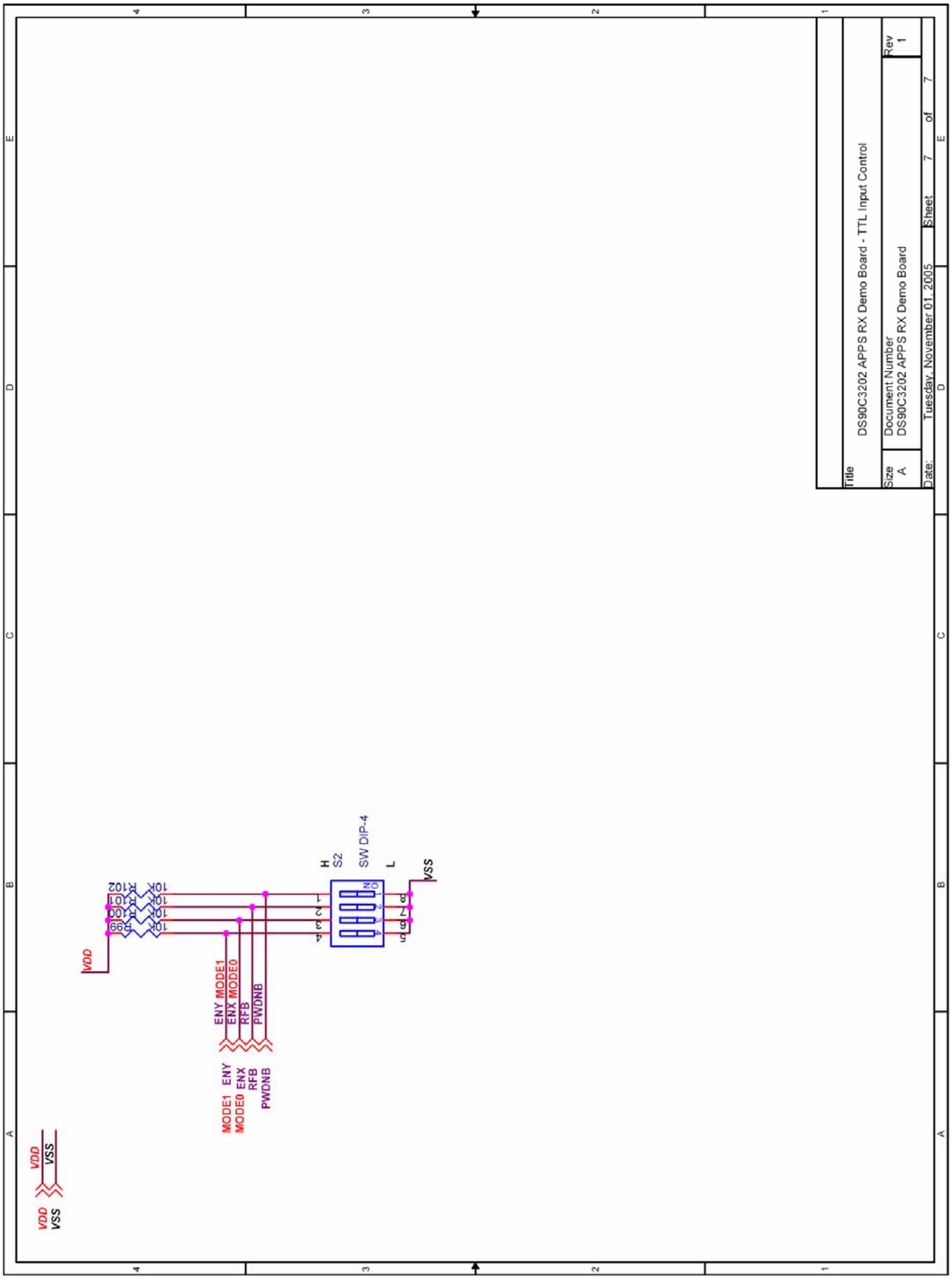

DS90C3202
Title
DS90C3202 APPS RX Demo Board - DS90C3202 Receiver
Size
A
Document Number
DS90C3202 APPS RX Demo Board
Rev
1
Date: Tuesday, November 01, 2005
Sheet 2 of 7
50 ohm single ended impedance traces
100 ohm differential impedance traces
LAYOUT NOTE: Mount JP1 near pin 1
LAYOUT NOTE: Mount JP2 near pin 2


LAYOUT NOTE:
NO IMPEDANCE REQUIREMENTS ON THESE TRACES.
LAYOUT NOTE:
LABEL -
INTERNAL SCL1
EXTERNAL SCL2
INTERNAL SDA1
EXTERNAL SDA2
SCL
SDA
JP77
JP78
IDC2X2_Unshrouded
USER NOTE:
1) To use onboard EEPROM (J1):
Jumper pin 1 to pin 2 on BOTH JP6 and JP7.
2) To use external EEPROM connector (JP18):
Jumper pin 3 to pin 4 on BOTH JP6 and JP7.
3) To connect onboard EEPROM to external EEPROM
Jumper pin 1 to pin 3 on BOTH JP6 and JP7.
4) To disconnect onboard EEPROM and external EEPROM
remove any jumpers BOTH JP6 and JP7.
Place near pin 8 of J1
C108 0.1uF
C109 0.01uF
C110 22uF
VDDE
VSSE
J6
DIP 4X2
A0 A1 A2 VSS SDA SCL PTC VDD
JP79
2-Pin Header
For write protection
LAYOUT NOTE:
Mount JP7 near pin 3
LAYOUT NOTE:
Mount JP7 near pin 4
JP75
JP76
3 pin Jumper
JP74
HEADER 4x1
USER NOTE:
External EEPROM connector.
LAYOUT NOTE:
LABEL -
A2 A1 A0
R109 10K
R108 10K
R107 10K
S1
SW DIP-3
LAYOUT NOTE:
1) When the switch is in the "ON" position the line is grounded;
when the switch is in the "OFF" position the line is pulled "HIGH".
2) Orient switch where "ON" is on the right-hand-side.
Title
DS90C3202 APPS RX Demo Board - EEPROM
Size A
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USER NOTES:
1) L1 - L11 option: pins 1 & 4 and pin 2 & 3 intentionally shorted. DO NOT populate if Tx board has L1- L11 populated.
L1 - L11 pads provided for evaluation purposes only.
L1 - L11 not required for operation of device.
LAYOUT NOTES:
1) 100 ohm differential matched trace length on RI(X-Y)(A-E), CLKIN and REFERENCE_N/P.
2) Minimum length
3) L1 - L11 pin 1/4 and pin 2/3 intentionally shorted.
DS90C3202 APPS RX Demo Board - LVDS Inputs
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LAYOUT NOTES:
1) Place R48 - R55 (zero ohm) as close as physically possible to associated pins on U1.
Title
DS90C3202 APPS RX Demo Board - Power and Decoupling
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Place near pin 16 of U1
Place near pin 33 of U1
Place near pin 65 of U1
Place near pin 95 of U1
Place near pin 100 of U1
Place near pins 113-114 of U1
Place near pins 5-6 of U1
Place near pin 25 of U1
Place near pin 2 of Tcon1
Place near pin 86 of U1
VDD
VSS
VDDE
VSSE
VDD1
VDD2
VDD3
VDD4
VDDL1
VDDL2
VDDP
VDDR1
VDDR2
VDDR3
F1
32VDC1A
F2
32VDC1A
BANANA


LAYOUT NOTE:
1) 50 ohm single-ended impedance requirement on these traces.
2) Matched trace length on RO[X-Y][A-E][0-6].
3) Minimum trace length on RO[X-Y][A-E][0-6].
4) Minimum trace capacitance on RO[X-Y][A-E][0-6].
5) open,0201 (R12- R82) intentionally shorted.
USER NOTE:
1) To use open,0201 resistor (R12- R82) pads, cut shorting trace before populating. R12 - R82 used for series damping resistor or providing resistor network divider (e.g. 10:1) capability.
VSS
Title
DS90C3202 APPS RX Demo Board - Series Termination and TTL Loading
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DS90C3202 APPS RX Demo Board - TTL Input Control
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A
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S2
SW DIP-4
H
L
VSS
VDD
10K
R99
R100
R101
R102
ENY MODE1
ENX MODE0
RFB
PWDNB
MODE1 ENY
MODE0 ENX
RFB
PWDNB
VDD
VSS